1400 W ZVS phase shift full bridge evaluation board

Using 600 V CoolMOS™ CFD7 and digital control by XMC4200

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About this document

Scope and purpose

This document describes the design and performance of a 1400 W ZVS Phase Shift Full Bridge (PSFB) evaluation board intended for use in the isolated HV DC-DC stage of an SMPS for server and industrial applications.

This is a high-performance example with a complete Infineon solution, including HV and LV power MOSFETs, controllers and drivers, demonstrating a very effective way to design the HV DC-DC stage of a server or industrial SMPS that fulfills the highest standards of efficiency and reliability. The overall best-in-class performance is achieved thanks to a mix of proper control techniques and best-in-class power device selection.

Key Infineon products used to achieve this performance level include:

- 600 V CoolMOS™ CFD7 SJ MOSFET
- Advanced dual-channel gate drive 2EDN7524F
- SR MOSFETs OptiMOS™ BSC026N08NS5
- XMC4200 microcontroller
- Flyback controller CoolSET™ ICE5QSAG + CoolMOS™ IPU80R4K5P7

Along with design information and documentation for the phase-shift converter, the reader will receive additional information on how the 600 V CoolMOS™ CFD7 behaves in ZVS PSFB applications and the associated benefits, how the high-performance magnetics design can be approached, and insights into how to develop the ZVS PSFB in similar power ranges adapted to specific requirements.

Intended audience

This document is intended for design engineers who wish to evaluate high-performance topologies for High Power (HP) SMPS converters, and develop an understanding of the design process and how to apply the ZVS PSFB design methods to their own system applications.

Note: *General knowledge about the soft-switching converter principle of operation is required for proper comprehension of the concepts covered in this paper.*

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1 Introduction

In today's AC-DC power supplies used in server and telecom base station applications, there is a growing need for high efficiency combined with high power density. The trade-off challenges in designing such a power converter are centered on the MOSFET and magnetics used in these HP designs. Soft-switching topologies provide the ability to switch at high frequencies, thereby reducing the size of the magnetics and also reducing the losses in the MOSFETs during switching transitions. The ZVS PSFB is one of the most common soft-switching topologies used in the applications listed above.

This application note predominantly discusses the benefits of the new 600 V CoolMOS™ CFD7 MOSFET in a ZVS PSFB topology. The 1400 W ZVS PSFB evaluation board is based on IPP60R170CFD7, and the benefits of CFD7 technology are clearly demonstrated here. The 1400 W board is the enhanced version of 800 W design explained in [15].

The highly innovative digital control scheme based on the XMC4200 helps to achieve very high efficiencies greater than 96.5 percent at half load and greater than 93 percent at light load, targeting the HV DC-DC stage of an 80Plus® Platinum® SMPS. Both Peak Current Mode (PCM) and Voltage Mode (VM) have been implemented and are available as possible options for the converter control. A Graphical User Interface (GUI) running in Windows has been designed in order to help the user interact with the demo board simply by using a PC/laptop through a serial communication (UART).

The innovative planar magnetic design and optimal layout enable a very compact form factor in the range of 50 W/inch^3 power density, and accommodate 1400 W in the same form factor as the 800 W version. This follows the modular approach currently very common in server and industrial SMPS to take advantage of economies of scale.

1.1 600 V CoolMOS™ CFD7 feature sets

The critical MOSFET parameters required in a ZVS PSFB converter are:

- Gate charge Q_g
- Output capacitance C_{oss}
- Body Diode (BD) Q_{rr}, t_{rr} and I_{rrm}
- On-resistance $R_{DS(on)}$

A typical loss breakdown in a ZVS PSFB converter ([1], [4]) will show that one of the main losses in the converter is due to the primary switching MOSFETs. We can further break down these losses within the MOSFETs and arrive at the conclusion that a significant percentage of losses at light-load (10 percent) operation is due to the MOSFET driving. The driving losses are directly proportional to the MOSFET gate charge Q_g. IPP60R170CFD7 has the lowest Q_g as compared to parts of a similar $R_{DS(on)}$ class. The low Q_g also enables fast switching. The conduction losses form a major percentage of losses within the MOSFET during full-load (100 percent) operation. They are directly proportional to the MOSFET $R_{DS(on)}$. The CFD7 technology has among the lowest $R_{DS(on)}$ per package available on the market, to enable high efficiency at full-load operation, without sacrificing any power density requirements. The benefits of reduction in Q_g and $R_{DS(on)}$ are directly visible in the efficiency improvements shown toward the end of this AN.

Another critical parameter for efficiency improvement in a ZVS PSFB topology is the MOSFET E_{oss}, which is the energy stored in its output capacitance. Lower MOSFET E_{oss} helps in selecting a smaller resonant inductor needed for the resonant tank in the bridge.

Other than the light-load and full-load efficiency benefits, the IPP60R170CFD7 also includes BD ruggedness, which is essential in topologies like the ZVS PSFB.

1.2 600 V CoolMOS™ CFD7 vs 650 V CoolMOS™ CFD2

In this paragraph the 600 V CoolMOS™ CFD7 benefits are compared to the older 650 V CoolMOS™ CFD2 technology. The CFD2 is the well-established predecessor of CFD7. The main features and benefits of the 650 V CoolMOS™ CFD2 are documented in the AN "650 V CoolMOS™ CFD2," released by Infineon in February 2011 [2]. In Figure 1 a quantitative comparison between IPP60R170CFD7 (green columns) and IPP60R190CFD2 (gray columns) is provided in order to show the improvements gained from the new 600 V CoolMOS™ CFD7 technology. The most relevant differences between key parameters of the two technologies are shown, with the corresponding impact on performance.

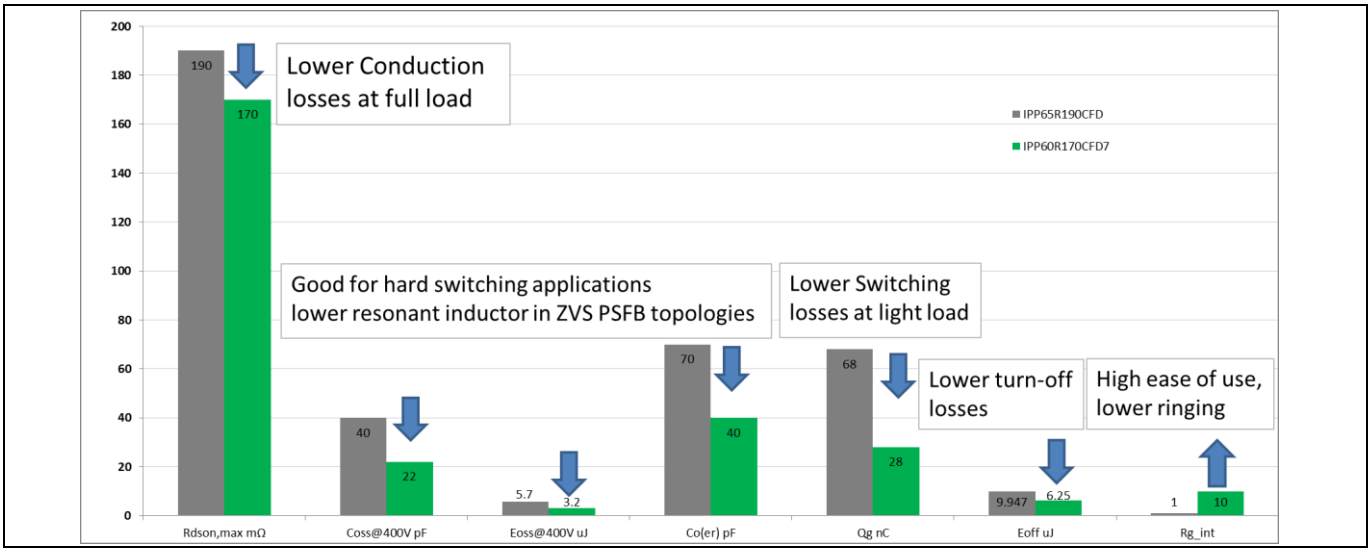


Figure 1 IPP60R170CFD7 vs IPP65R190CFD – key datasheet parameter comparison and key benefits

Trade-offs involving adjustments of delay times, dimensioning of the resonant inductance and impact of $R_{G(ext)}$ optimization of primary-secondary MOSFETs delays are going to be explained in detail in this AN. General guidelines for a ZVS phase shift design methodology are available in previous AN "ZVS PSFB CFD2 optimized design," released by Infineon in March 2013 [1]. In the current AN we also focus on the innovative digital control and planar magnetic design.

The main focus of this AN is on the waveforms analysis in a "real" application board, which has similar power densities as the best commercial variants available in the market. Digital control technique and the design trade-offs involving the ZVS phase-shift topology, such as placement of the clamp diodes, Current Sensing (CS) and planar magnetic design, are explained in detail in the subsequent sections.

The measurement results are available in the last section of this AN. The high efficiency benefits of IPP60R190CFD7 are compared with IPP65R190CFD and some relevant competitors.

2 Design concept

The demo board has been designed according to the typical requirements of the HV DC/DC stage of a server or industrial SMPS:

- Input voltage range 350 V DC–410 V DC
- Nominal input voltage 400 V DC
- Output voltage 12 V ±4 percent
- Max. output current/power 117 A/1400 W
- Efficiency: greater than or equal to 93 percent at 20 percent load, greater than or equal to 96.5 percent at 50 percent load, greater than or equal to 96 percent at 100 percent load (target: 80Plus® Platinum® standard)
- 1U form factor
- Power density = 50 W/inch^3
- f_{sw} = 100 kHz

2.1 ZVS PSFB converter

The ZVS PSFB is one of the most popular soft-switching topologies in use in HP SMPS applications. Introduced in the 1990's [5], it immediately gained popularity in the power electronic designers community due to its relatively smooth way of minimizing switching losses even without using a fully resonant operation, thus avoiding all the possible pitfalls related to the resonant approach.

The only trouble occurred when this toplogy first began to be used, as a result of some critical operating conditions, like output short-circuit, especially starting from no-load operation. In fact some apparently "unexplainable" failures started happening around the world, mainly related to the unavoidable use of the intrinsic MOSFET BD [6]. Nowadays these conditions are fully understood: the use of appropriate control techniques, combined with the selection of proper HV MOSFET in the full bridge helps prevent any problems from the conditions described above.

More precisely, the advent of the CoolMOS™ technology, with a vertical structure based on the superjunction (SJ) concept, has removed all possible failure mechanisms linked to the parasitic BJT ignition, one of the root causes of the initial trouble with this topology (see [7] for more details).

Moreover, it has ben demonstrated that a MOSFET with fast BD is able to intrinsically prevent any problem in those conditions (see [1] for more details).

The 600 V CoolMOS™ CFD7 technology provides a fast and rugged BD, definitely suitable for this topology, as long as an excellent switching Figure of Merit (FOM), in order to allow reliable operation in high-performance converters.

2.1.1 Principle of operation

The ZVS PSFB topology principle of operation has already been described in [1]. For the reader's convenience, Figures 2 and 3 give a quick recap of the fundamental steps.

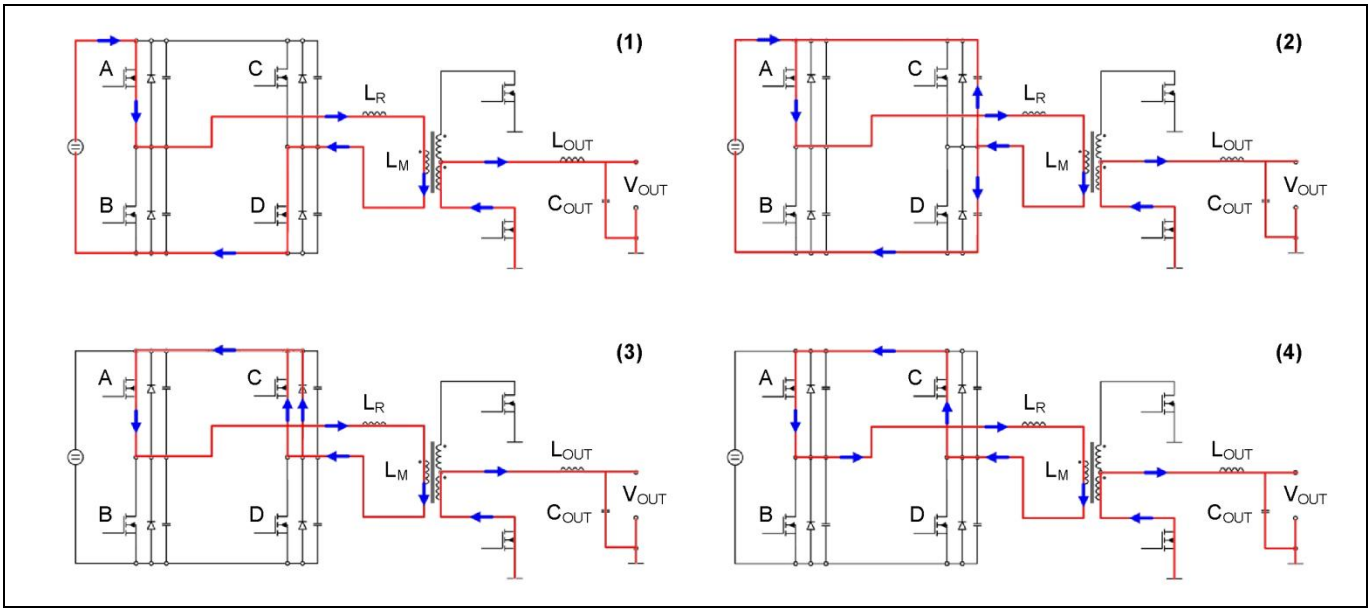


Figure 2 ZVS PSFB principle of operation: phases 1–4

1. Power transfer phase: MOSFETs A and D are turned on and the current flows as shown in the diagram. During this phase the primary current is rising according to the value of the total primary inductance.
2. The second phase is responsible for the ZVS of MOSFET C. In order to reach a zero-voltage turn-on, the energy stored in the resonant inductance is used to discharge the output capacitance of MOSFET C and charge the output capacitance of MOSFET D.
3. After the output capacitance of MOSFET C is discharged, the current is commutating to the BD of MOSFET C.
4. MOSFET C is actively turned on and the current is flowing through the channel and not through the BD any more. This phase is also called the “freewheeling phase.”

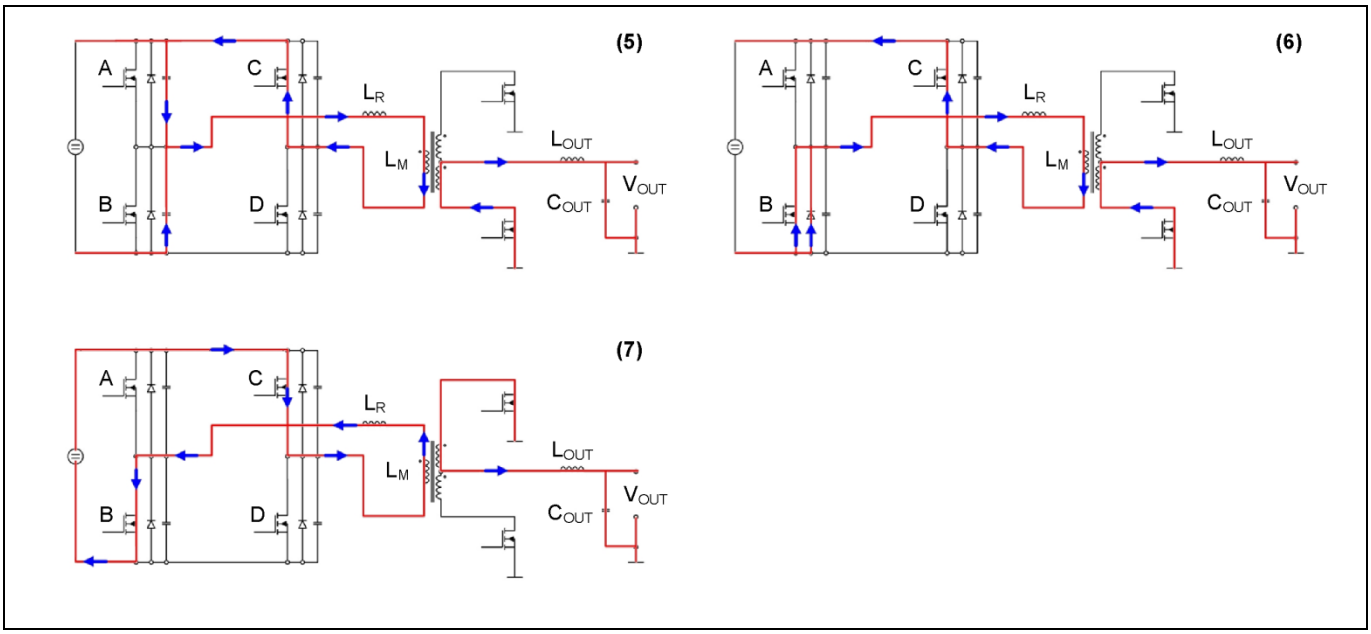


Figure 3 ZVS PSFB principle of operation: phases 5–7

5. In order to start a new power transfer phase MOSFET B is turned on. This phase is achieved in the same way as phase 2 by turning off MOSFET A. The output capacitance of MOSFET A is charged and the output capacitance of MOSFET B is discharged before actively switching on the MOSFET.
6. The BD conduction time of MOSFET B, which is visible in this phase, should also be reduced to a minimum as in phase 3.
7. MOSFET B is actively turned on, the current changes its direction and the next power transfer phase starts.

Figure 4 shows the control signals applied to the four MOSFETs of the bridge.

(1) and (7) are power transfer phases, whose duration defines the total effective on-time (and thus the duty cycle), which is given by the overlapping conducting period of the MOSFET on the same diagonal (A-D and B-C). The time interval (2)-(3) and (5)-(6) are also called dead times: they represent the time between the turn-off and turn-on of the MOSFETs on the same leg. They must be set long enough in order to achieve ZVS turn-on.

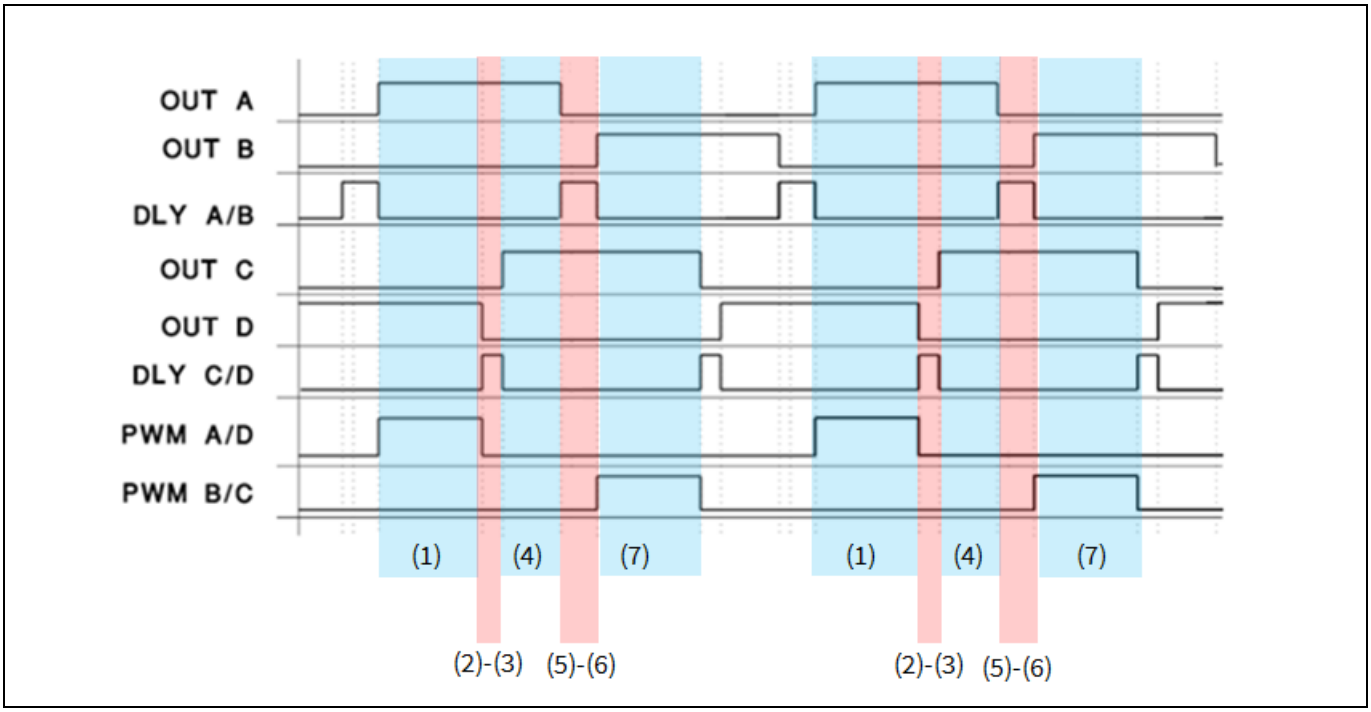


Figure 4 Control signals in the ZVS PSFB operation

It can be observed that the duration of these two times is not equal: the one applied to the C-D leg is lower than the one applied to the A-B leg. This is because C-D starts a ZVS transition after a power transfer phase, so with a higher amount of resonant energy available compared to A-B, which starts the transition before the power transfer.

For this reason C-D is commonly called the “lagging leg” and A-B the “leading leg.”

Thus, assuming the same MOSFETs (same C_{oss}) are used in the two legs, the time needed to discharge the output capacitance is obviously lower for the lagging leg compared to the leading leg.

Further and more detailed explanations of the ZVS PSFB topology operation and control, including the secondary Synchronous Rectification (SR), are reported in the section 4 of this document.

2.2 Planar transformer technique

The main transformer has been designed using a planar structure. This development has been done by Infineon in cooperation with the company Payton Planar Magnetics Ltd.

Planar technology is ideal for producing highly interleaved transformers. This high interleaving, if used correctly, can reduce leakage inductance and significantly reduce the proximity effect losses in the transformer.

As switching frequency increases, the need for reducing proximity effect losses becomes more important.

With its superior conduction cooling and highly repeatable results, planar technology is the best suited to most high-efficiency high-frequency transformer designs.

As with all technologies, it is imperative to use it accurately in order to maximize its performance. That is why custom-made designs are a crucial part of any power supply design aimed at maximizing efficiency and reducing size. Only a tailored solution will be able to unlock the full potential of any technology.

By combining the strength of planar technology with wire-wound design, Payton Planar products strive to maximize efficiency and reduce size while meeting all of the power supply designer's requirements.

See [14] for more details about planar transformers in soft-switching DC-DC converters.

2.2.1 Concept

In the unique transformer design for the 1400 W ZVS PSFB demo board a special multi-layer PCB has been used for the primary winding, with thick copper winding, and stamped copper lead frames for the secondary side. The special PCB design has been chosen in order to achieve a high number of turns and at the same time meet the high insulation requirements. Using a PCB for winding also improves the reliability and repeatability of the winding.

Copper-stamped lead frames were used for the secondary side. The thick copper windings made it possible to handle the high currents on the secondary side of the transformer as in a typical server or industrial 12 V output SMPS.

In order to achieve a high interleaving count and improve proximity losses, the transformer has three separate unique PCB boards. Primary windings were sandwiched between the secondary lead frames, which helps to achieve very low proximity losses.

In order to reach the leakage inductance required to energize the ZVS behavior, without increasing proximity losses, an integrated inductor was designed on the top of the transformer. The integrated inductor has a magnetic flux in the opposite direction to the transformer magnetic flux, and in this way core losses can be reduced. This construction also saves on board space and height.

The inductor cannot be interleaved as it has only one winding, so this has been done with litz wire to improve its efficiency at high frequency. The inductor lead wires are connected through the transformer PCB. This connection combines two magnetic parts into one module with low losses and high leakage inductance value. This helps reduce the number of components, as the transformer and inductor can be considered as one module.

Figure 5 shows the concept: the detailed spec of the the transformer is available in section 3.3.1.

In conclusion, our planar concept is the best way to combine high power density, reduced AC and core losses, high current capability and very good reproducibility in mass production: all are important requirements in HP and high-performance SMPS for server and industrial applications.

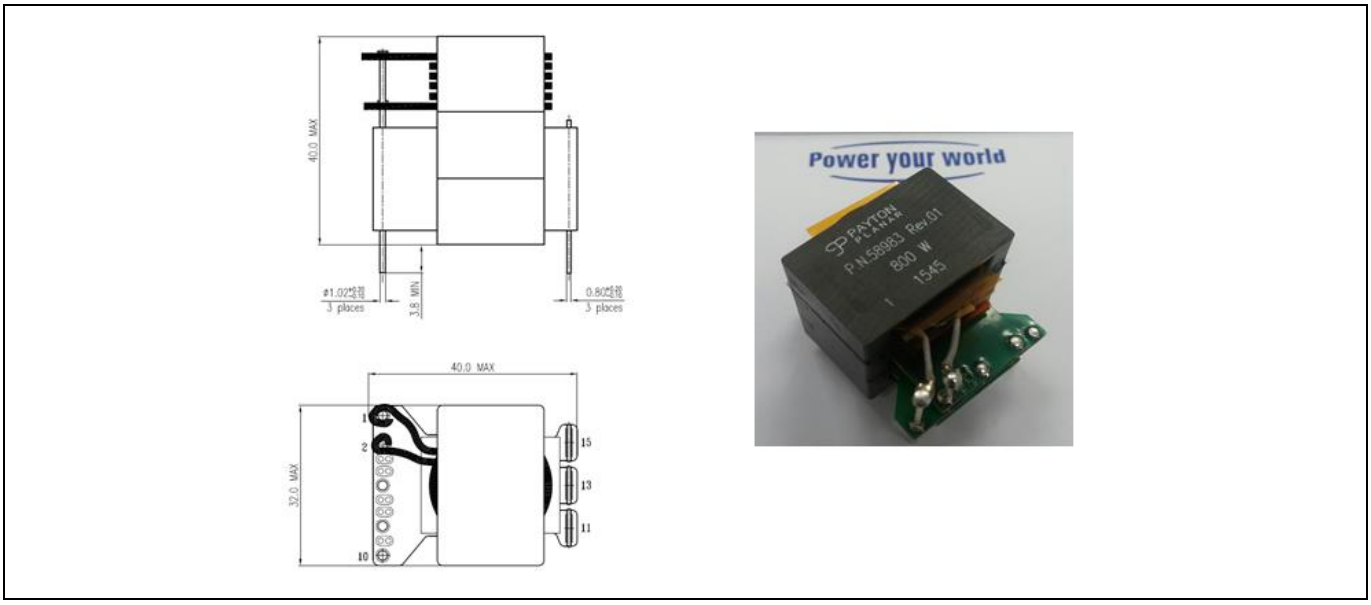


Figure 5 Main transformer: planar stacked structure

3 Board description

Figure 6 gives an overview of the demo board components.

It consists of a main power board (where the main transformer and all power components are assembled) and three daughter cards: the digital control, the SR and the auxiliary converter cards, which can be easily identified in Figure 6 below.

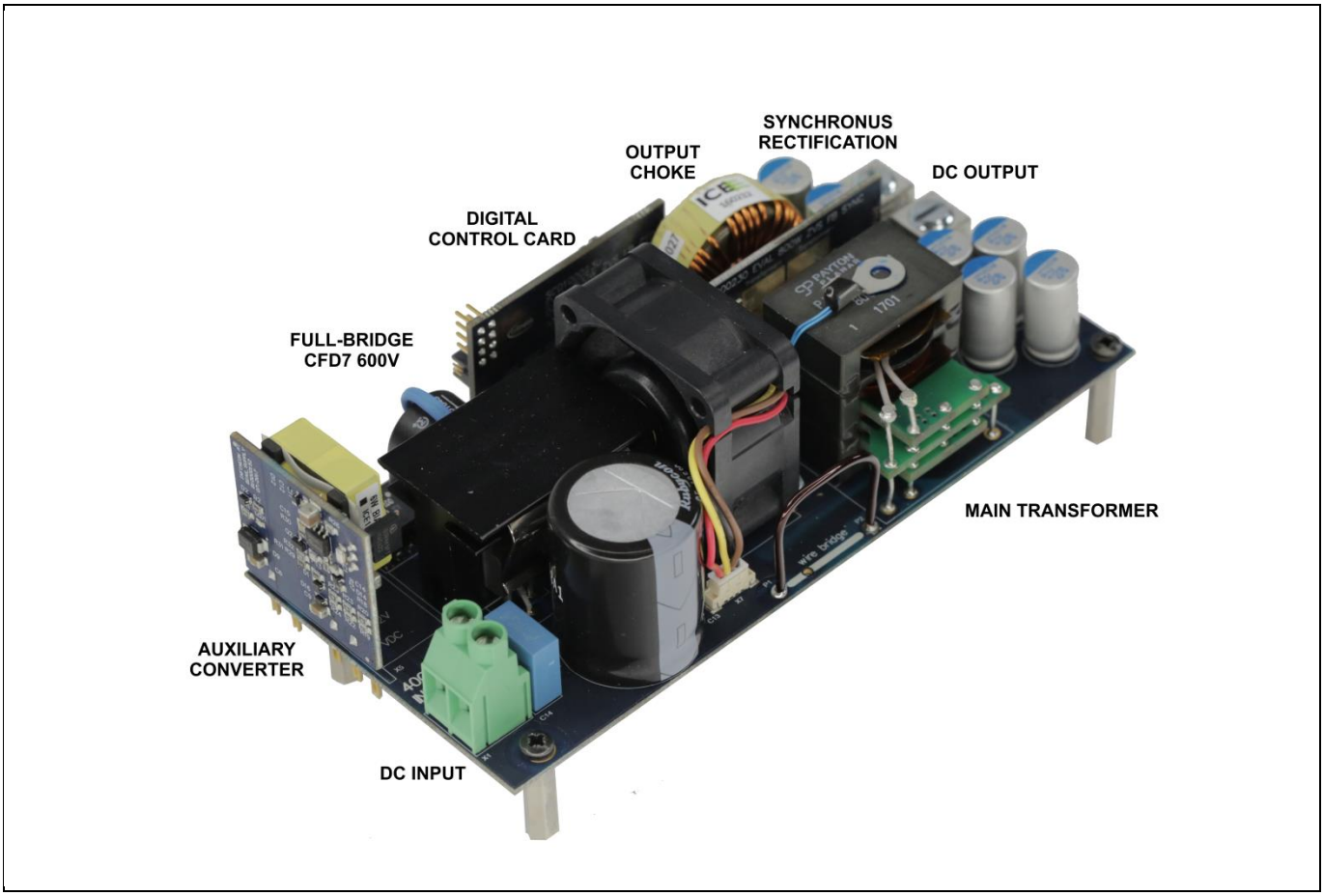


Figure 6 Board overview

3.1 Infineon components

3.1.1 Primary HV MOSFETs 600 V CoolMOS™ CFD7

CoolMOS™ is a revolutionary technology for HV power MOSFETs, designed according to the SJ principle and pioneered by Infineon Technologies. The latest 600 V CoolMOS™ CFD7 is the successor to the CoolMOS™ CFD2 series and is an optimized platform tailored to target soft-switching applications such as PSFB ZVS and LLC. Resulting from reduced gate charge (Q_g), best-in-class reverse recovery charge (Q_{rr}) and improved turn-off behavior, 600 V CoolMOS™ CFD7 offers the highest efficiency in resonant topologies. As part of Infineon's fast BD portfolio, this new product series combines the advantages of a fast-switching technology together with superior hard-commutation robustness, without sacrificing easy implementation in the design-in process. The 600 V CoolMOS™ CFD7 technology meets highest efficiency and reliability standards and furthermore supports high power density solutions. Altogether, 600 V CoolMOS™ CFD7 makes resonant switching topologies more efficient, more reliable, lighter and cooler.

Features

- Ultra-fast BD
- Low gate charge (Q_g)
- Best-in-class reverse recovery charge (Q_{rr})
- Improved MOSFET reverse diode dv/dt and di/dt ruggedness
- Lowest FOM $R_{DS(on)}$*Q_g and $RDS_{(on)}$*E_{oss}
- Best-in-class $R_{DS(on)}$ in SMD and THD packages
- Qualified for industrial-grade applications according to JEDEC (J-STD20 and JESD22)

Benefits

- Excellent hard-commutation ruggedness
- Highest reliability for resonant topologies
- Highest efficiency with outstanding ease-of-use/performance trade-off
- Enabling increased power density solutions

Applications

- Suitable for soft-switching topologies
- Optimized for PSFB ZVS and LLC stages in server, telecom and EV charging applications

3.1.2 Advanced dual-channel gate drive 2EDN7524

The fast dual-channel 5 A non-isolated gate driver is an advanced dual-channel driver optimized for driving both standard and SJ MOSFETs, as well as GaN power devices, in all applications in which they are commonly used. The input signals are TTL compatible with an HV capability of up to 20 V and down to -5 V. The unique ability to handle -5 V DC at input pins protects the IC inputs against ground bounce transients.

Each of the two outputs is able to sink and source up to 5 A current utilizing a true rail-to-rail stage, which ensures very low impedances of 0.7 Ω up to the positive and 0.55 Ω down to the negative rail respectively. Very low channel-to-channel delay matching is implemented, typically 1 ns, which enables the double source and sink capability of 10 A by paralleling both channels.

Different logic input/output configurations guarantee high flexibility for all applications; e.g. with two paralleled switches in a boost configuration. The gate driver is available in three package options: PG-DSO-8, PG-VDSON-8 and PG-TSDSO-8-X (size minimized DSO-8).

Main features

- Industry-standard pin-out
- Two independent low-side gate drivers
- 5 A peak sink/source output driver at V_{DD} = 12 V
- True low-impedance rail-to-rail output (0.7 Ω and 0.5 Ω)
- Enhanced operating robustness due to high reverse current capability
- -10 V DC negative input capability against GND-bouncing
- Very low propagation delay (19 ns)
- Typ. 1 ns channel-to-channel delay matching
- Wide input and output voltage range up to 20 V
- Active low output driver even on low power or disabled driver
- High flexibility through different logic input configurations
- PG-DSO-8, PG-VDSON-8 and TSSOP-8 package
- Extended operation from -40°C to 150°C (junction temperature)
- Particularly well suited to driving standard MOSFETs, SJ MOSFETs, IGBTs or GaN power transistors

3.1.3 SR MOSFETs OptiMOS™ BSC026N08NS5

OptiMOS™ 5 80 V, Infineon's latest generation of MV power MOSFETs, are especially designed for SR in telecom and server power supplies. In addition, these devices can also be utilized in other industrial applications such as solar, LV drives and adapters.

The OptiMOS™ 5 80 V MOSFETs yield designs with lowest SR losses: the extremely low $R_{DS(on)}$ allied with extremely low output (Q_{oss}), reverse recovery (Q_{rr}) and gate (Q_g) charges reduce not only conduction losses but also switching losses.

The OptiMOS™ 5 80 V SR MOSFET low output and reverse recovery charges drain less energy from the input voltage source, through the isolation transformer, contributing to an increase in the converter efficiency. Moreover, these low charges also store less energy in the isolation transformer leakage inductance and in the primary-side resonant inductor, yielding not only an over-shoot with low energy on the SR MOSFET being blocked, but also low recirculated current through the primary-side inductor clamping diodes, which also contributes positively to the efficiency of the converter.

Finally, the OptiMOS™ 5 80 V MOSFET low gate charge alleviates the burden on the SR driver circuitry, especially in HP designs, like this one, which employ many paralleled SR MOSFETs.

Summary of features

- Optimized for SR
- Ideal for high switching frequency
- Optimized $C_{oss} \times R_{DS(on)}$ FOM

Benefits

- Highest system efficiency
- Reduced switching and conduction losses
- Less paralleling required
- Increased power density
- LV over-shoot

3.1.4 XMC4200

The XMC4200 combines Infineon's leading-edge peripheral set with an industry-standard ARM® Cortex®-M4F core.

The control of SMPS is a strong focus for XMC™ microcontrollers, where users can benefit from features such as smart analog comparators, high-resolution Pulse Width Modulation (PWM timers and the ARM® Cortex®–M4F DSP instruction set, including floating-point or high-precision analog-to-digital converter.

As a key feature it offers a high-resolution PWM unit with a resolution of 150 ps. This unique peripheral makes it especially suitable for digital power conversion in applications such as solar inverters as well as SMPS and Uninterruptible Power Supplies (UPS).

The XMC4200 is supported by Infineon's integrated development platform DAVE™, which includes an IDE, debugger and other tools to enable fast, free-of-charge and application-oriented software development.

Summary of XMC4200 key features

- ARM® Cortex®-M4F, 80 MHz, including single-cycle DSP MAC and Floating Point Unit (FPU)
- CPU frequency: 80 MHz
- High ambient temperature range: -40°C to 125°C
- Wide memory size options: up to 512 kB of Flash and 80 kB of RAM
- HRPWM (High Resolution PWM) allowing PWM adjustment in steps of 150 ps
- 12-bit ADC, 2 MSample/s; flexible sequencing of conversions including synchronous conversion of different channels
- Fast and smart analog comparators offer protections such as Over Current Protection (OCP), including filtering, blanking and clamping of the comparator output; a 10-bit DAC with a conversion rate of 30 MSamples/s provides an internal reference for the comparators that can be configured to be a negative ramp for slope compensation purposes
- A flexible timing scheme due to CCU timers and HRPWM; these timers allow the creation of almost any PWM pattern and accurately synchronize PWM signals with ADC measurements
- Interconnection matrix to route different internal signals from one peripheral to another; for example, the comparator output can connect to a PWM timer to indicate an OCP event and immediately switch off the PWM output
- Communication protocols supported, including USB, UART, I^2C, SPI

3.1.4.1 CCU8-PWM generation

The CCU8 is a multi-purpose timer unit for signal monitoring/conditioning and PWM signal generation. It is designed with repetitive structures with multiple timer slices that have the same base functionality. The internal modularity of the CCU8 translates into a software-friendly system for fast code development and portability between applications [8].

Each CCU8x has four 16-bit timer slices, CC8y (y = 3-0), which can be concatenated up to 64-bit.

A slice has:

- One timer
- Four capture registers
- One period register
- Two compare registers

Its numerous key features for a flexible PWM generation scheme make it the perfect peripheral for PWM generation in SMPS. Some features include:

- Each timer slice of the CCU8 can operate in center-aligned or edge-aligned mode
- Additional operation modes like single-shot, counting or dithering modes are also available
- Complementary PWM signal generation with dead time
- HW asymmetric PWM generation for multi-channel/multi-phase pattern generation with parallel updates
- Additional external controllable functions give another degree of PWM manipulation (e.g. timer gate, timer load, timer clear, etc.)
- HW TRAP generation
- Both the period and compare registers have shadow registers
- Each slice can work independently and in different modes, and still be synchronized to other CCU8 slices

Due to all these features the CCU8 timer slices are used to drive the PSFB 800 W. See Figure 7 for some examples of CCU8 usage.

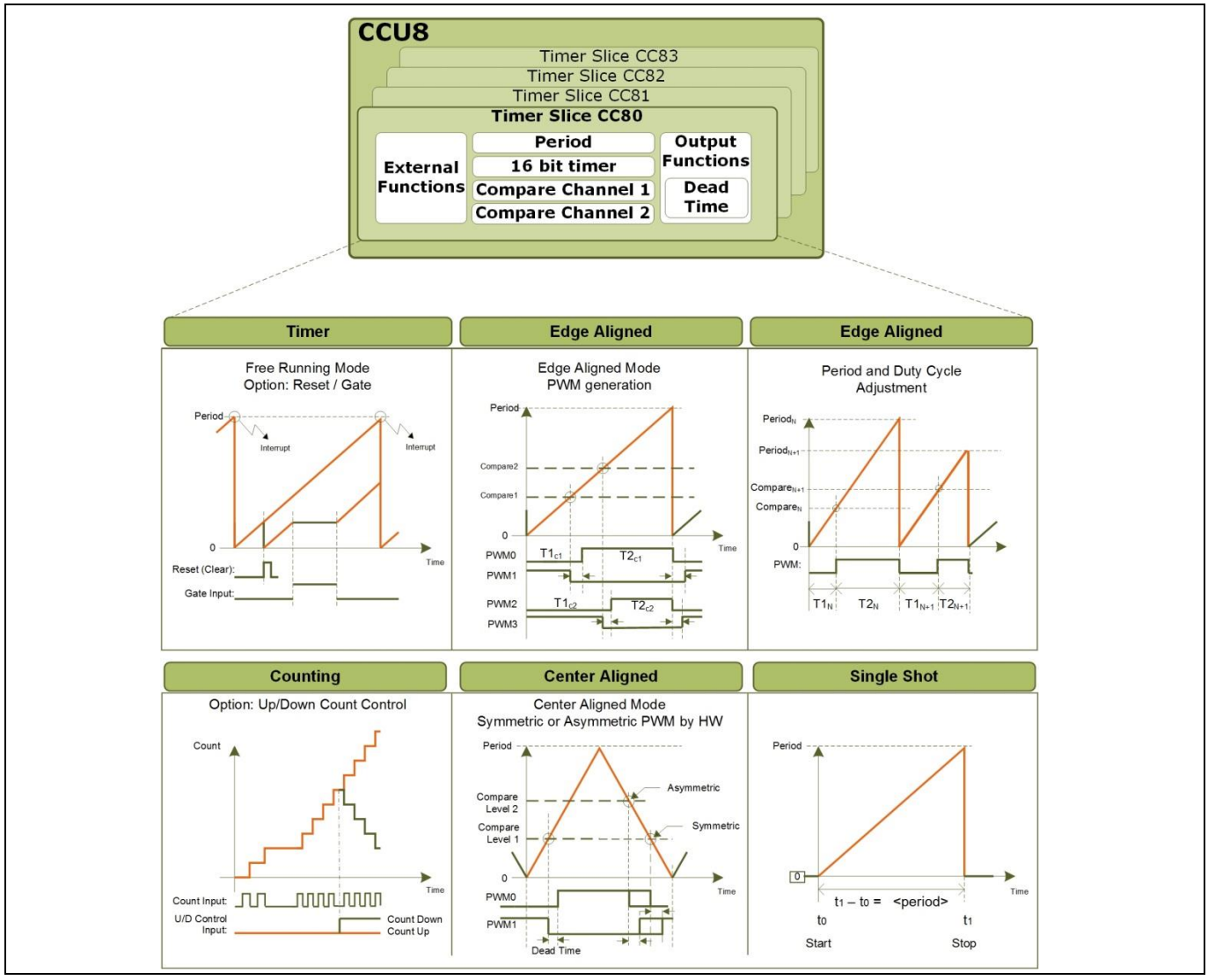


Figure 7 CCU8 flexible PWM generation scheme

3.1.4.2 HRPWM generation

The HRPWM generator (150 ps) is an essential module, for cutting-edge and optimized SMPS application development [8].

The XMC42xx devices offer High Resolution Channel (HRC) generation. The HRPWM is used together with CCU8 slices.

The enhanced PWM resolution is performed by means of an insertion that shortens or lengthens the original pulse width of the CCU8 slice output pulse in steps of 150 ps. It can offer a resolution of 10 bits up to 6 MHz PWM. A dynamic dead-time insertion feature is available in the HRPWM path.

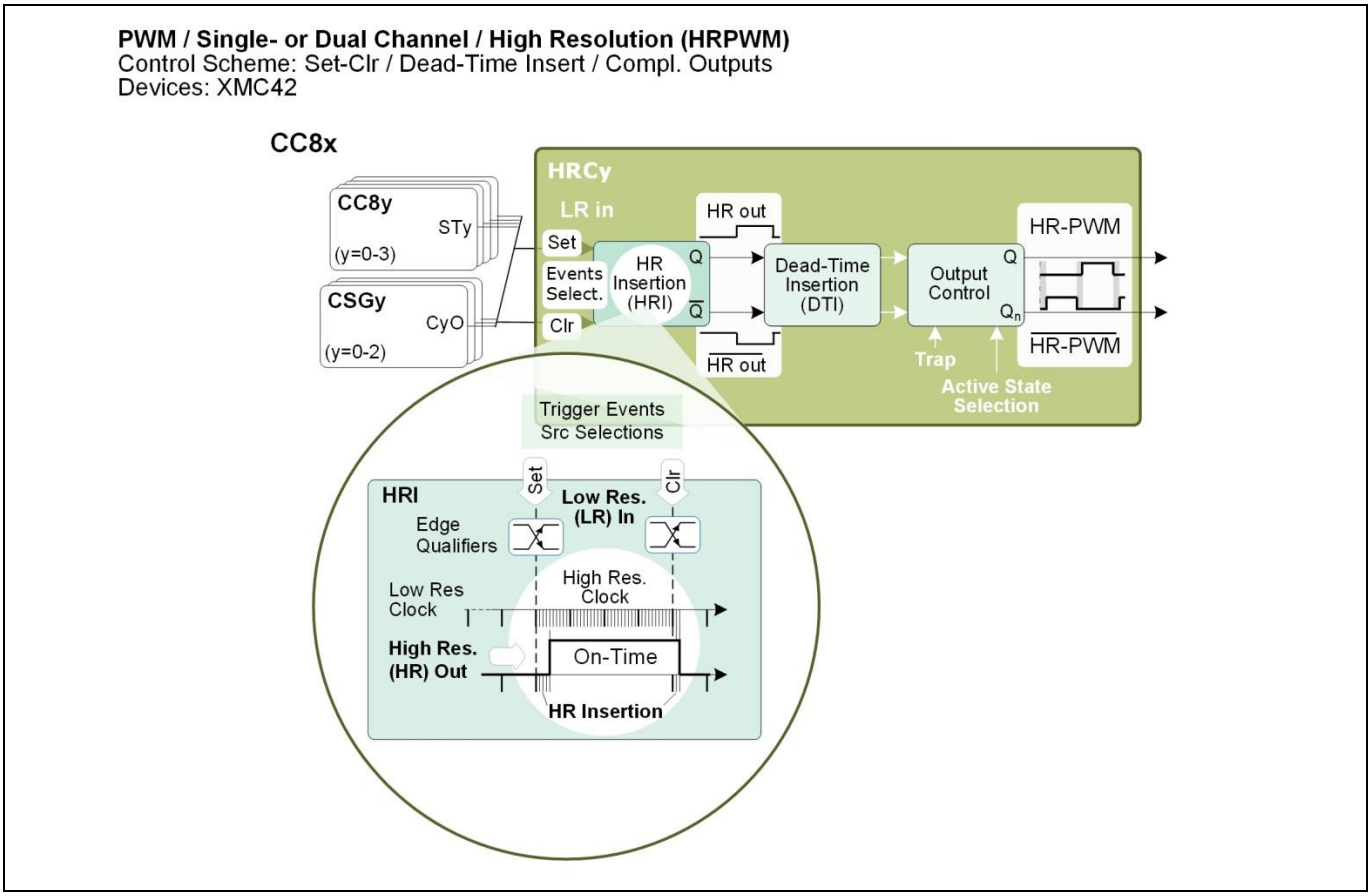


Figure 8 High-resolution channel

3.1.4.3 Voltage and current sensing-VADC

Input voltage, output voltage, and inductor current and all necessary signals to control a power converter can be monitored via Versatile Analog-to-Digital Converter (VADC) channels in XMC™ [8].

The functionalities of VADC that are useful for digital power control are as follows:

- Automatic scheduling of complex conversion sequences with priority for time-critical conversions
- Synchronous sampling of several analog signals
- Independent result registers, selectable for 8/10/12 bits, with 16 steps FIFO
- Sampling rates up to 2 MHz (up to 1 MHz for the XMC1000 family)
- FIR/IIR filter with selectable coefficients plus accumulation

The VADC module is intelligently connected to other peripherals, like PWM generation modules, in the MCU. This provides an accurate sampling point for real-time applications where the conversion of the analog signals must be done in a deterministic way.

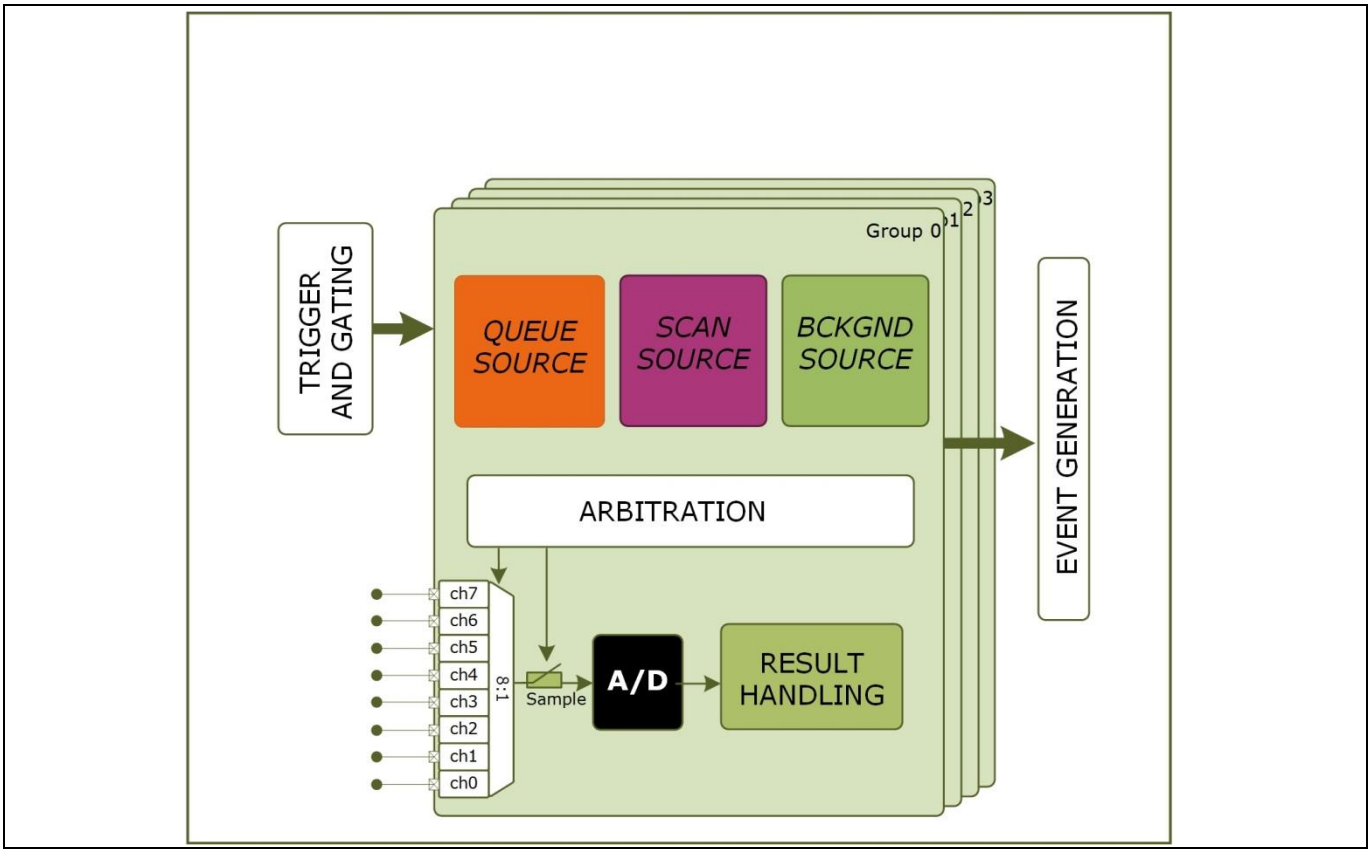


Figure 9 VADC schema

3.1.4.4 Comparator and Slope Generator (CSG) – XMC4200 MCU

With three high-speed comparators and a hardware slope, it is possible to address several power-conversion topologies with reduced software interaction. The CSG consists of essential interaction factors for several control techniques (see Figure 10); an analog high-speed comparator ~20 ns that can be used to monitor:

- Coil current for current protection or Peak Current Mode Control (PCMC)
- Voltage outputs for protections
- Slope generator with high-speed DAC (~30 Msample/s) that can be used to:
  - Reference control for the comparator
  - Insert a decrementing or incrementing ramp to the comparator for PCMC
- Filtering and blanking capabilities to avoid current commutation spikes to pass to the comparator

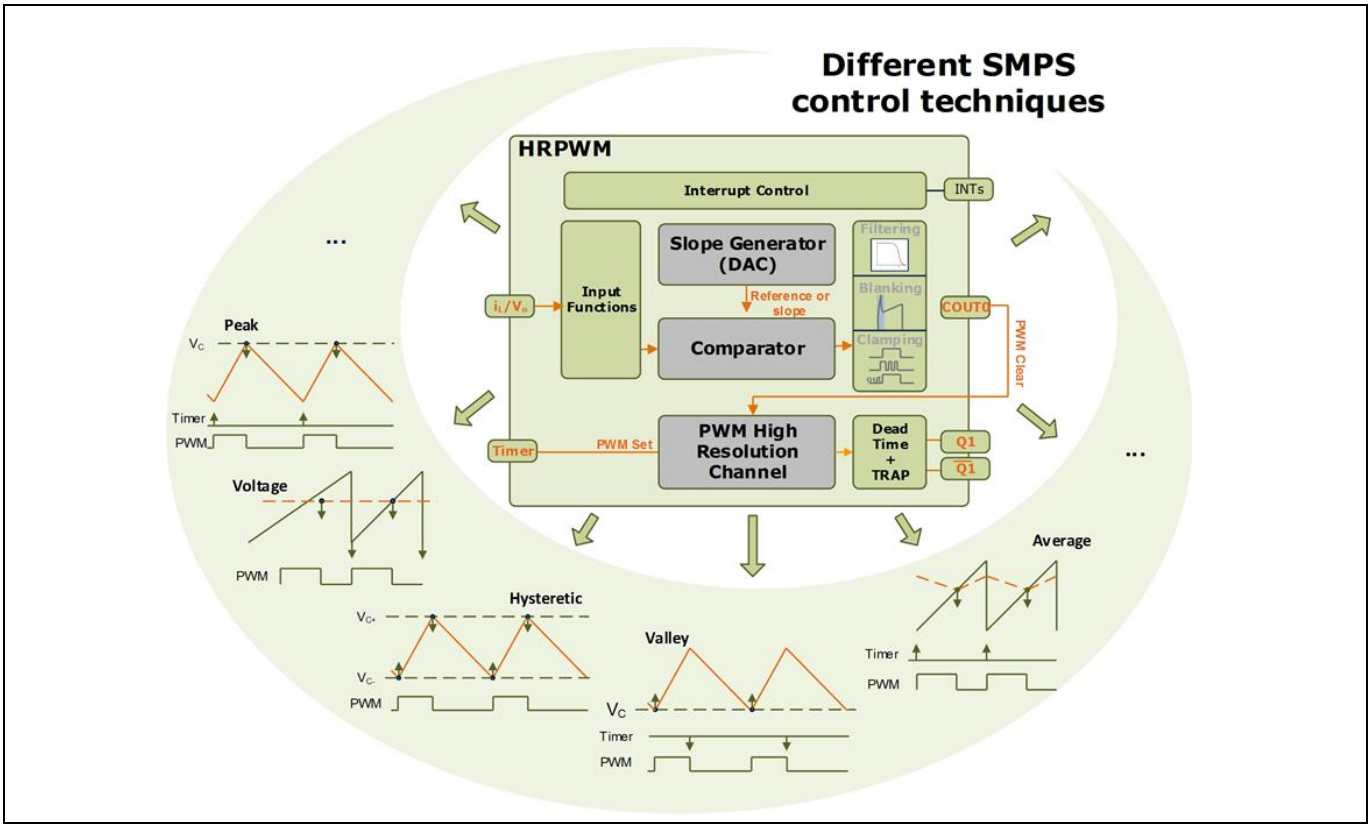


Figure 10 Using the CSG together with the HRC for implementing different SMPS control techniques

3.1.4.5 Event Request Unit (ERU)

The Event Request Unit (ERU) module can be used to expand the point-to-point connections of the device: ports-to-peripherals, peripherals-to-peripherals and ports-to-ports. It also offers configurable logic that allows the generation of triggers, pattern detection and real-time signal monitoring [8].

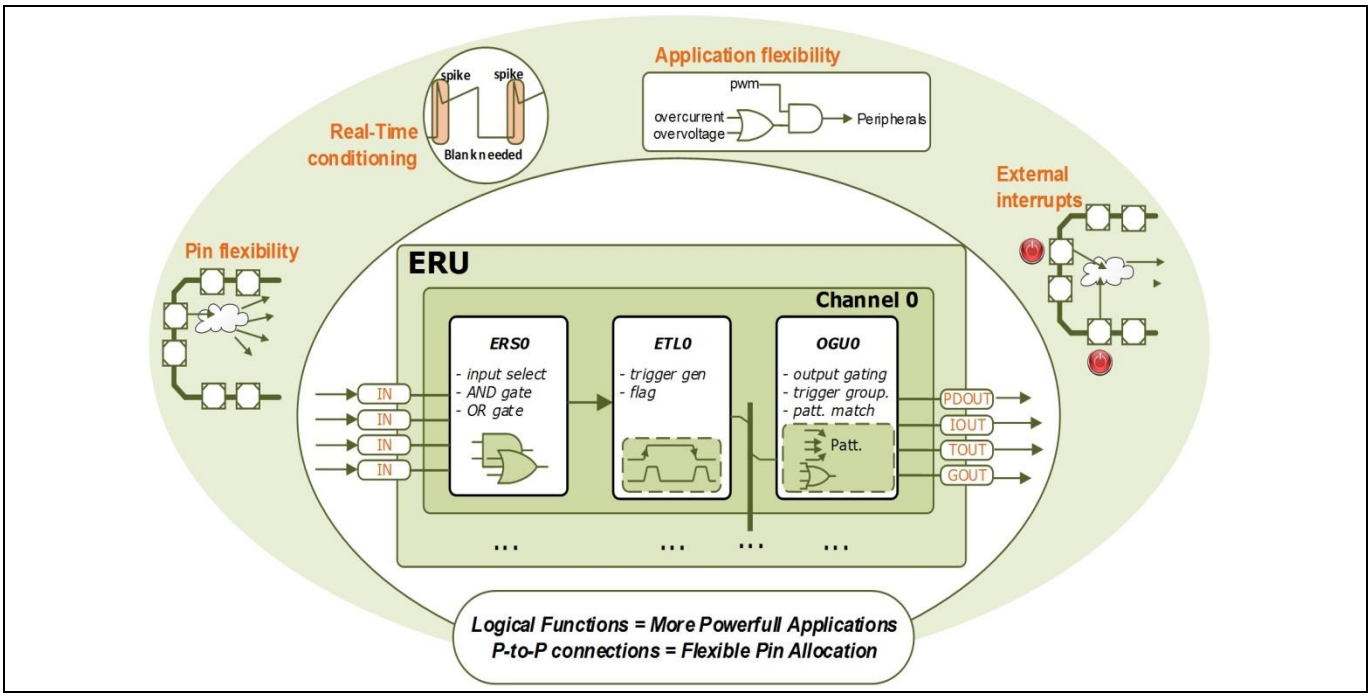


Figure 11 XMC™ peripheral interconnections through the ERU

3.1.5 New 6 W bias based on ICE5QSAG and IPU80R4K5P7

This board provides the power to the system primary and secondary sides in order to power the controller and gate drivers for the various boards. This has been designed to be a replacement for an existing bias module, so it was required to meet the same form factor or preferably be smaller while improving the bias efficiency. We acheieved this result by using the latest Infineon devices: the ICE5QSAG controller and a 800 V CoolMOS™ P7 SJ MOSFET IPU80R4K5P7. The stand-alone MOSFET was used to give flexibility and also to act as a test platform for future Infineon MOSFETs. This new demo board design resulted in a 10.4 percent efficiency improvement with a 6 W load and 25 percent improvement in efficiency with a 1 W load. The form factor was also reduced, with a 2.7 mm reduced PCB height, a 4.0 mm reduced PCB length and a 1.4 mm reduced PCB width. Form factor and efficiency were the focus, so this is not a cost-optimized design. The discrete MOSFET can also be replaced with a CoolSET™. This was done to allow flexibility for testing new Infineon devices in different $R_{DS(on)}$ values and voltage classes. A part like ICE5QR4780AZ would have the equivalent CoolMOS™ device integrated. The board has a 12 V output that is regulated on the primary side, and the secondary side is an unregulated 12 V output. It is designed for the full 6 W of operation from 350 V DC – 440 V DC, while it is capable of 1 W starting at 70 V DC. This is because when the system is starting up it only has to power the gate drivers and the controllers. During normal operation once the PFC is running the fan needs to also run, which is a majority of the load that the bias needs to power during steady-state operation. The strategies used in this converter, QR operation, removing the snubber network, and an interleaved transformer design can also be applied to other low-power Flyback designs for an overall improvement in performance.

The pictures below show the populated top and bottom layers of the new 6 W bias board.



Figure 12 Front and rear view of the 6 W bias board

The benefits of the new approach are visible in the following picture, where the overall dimensions are compared with the old version:

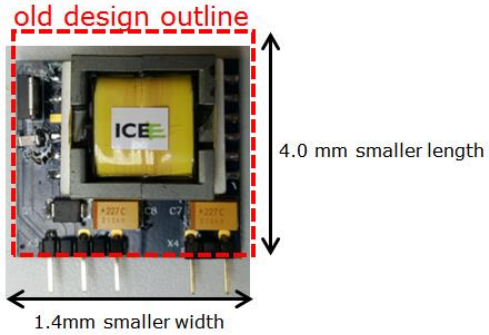


Figure 13 6 W bias board dimensions

Further details on the 6 W bias board design are available in [16].

3.2 Board schematics

3.2.1 Main converter

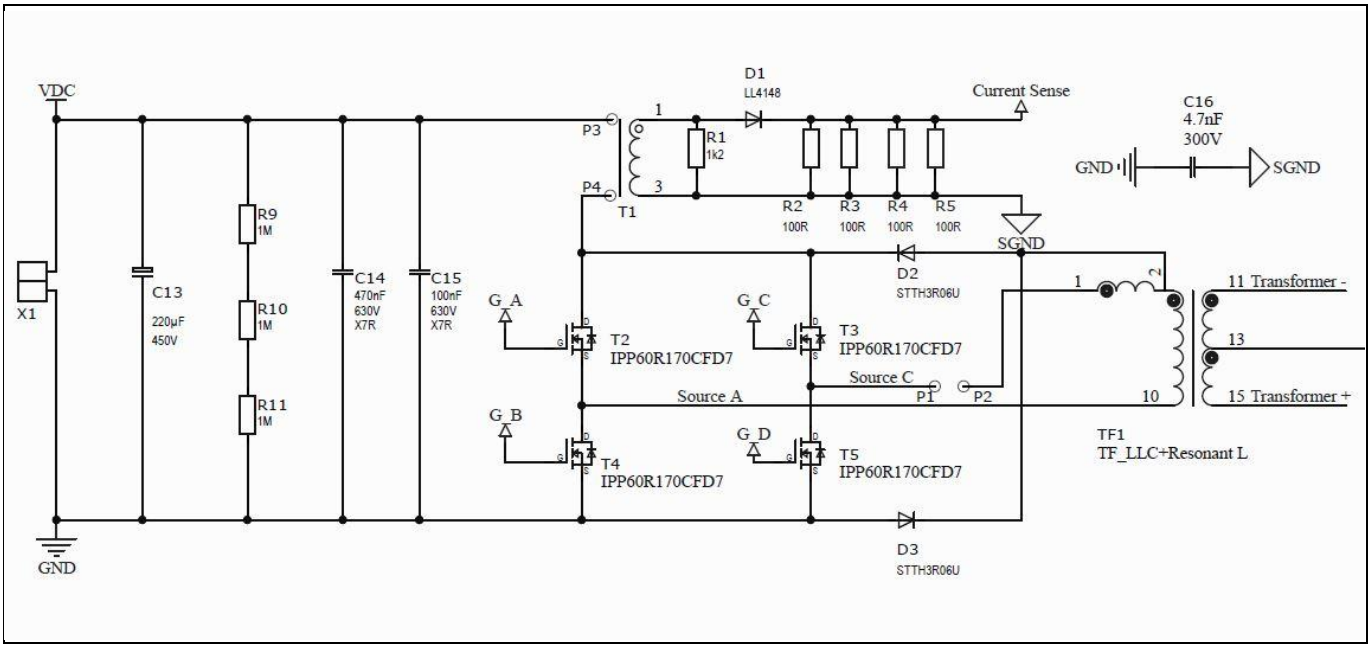


Figure 14 Primary side

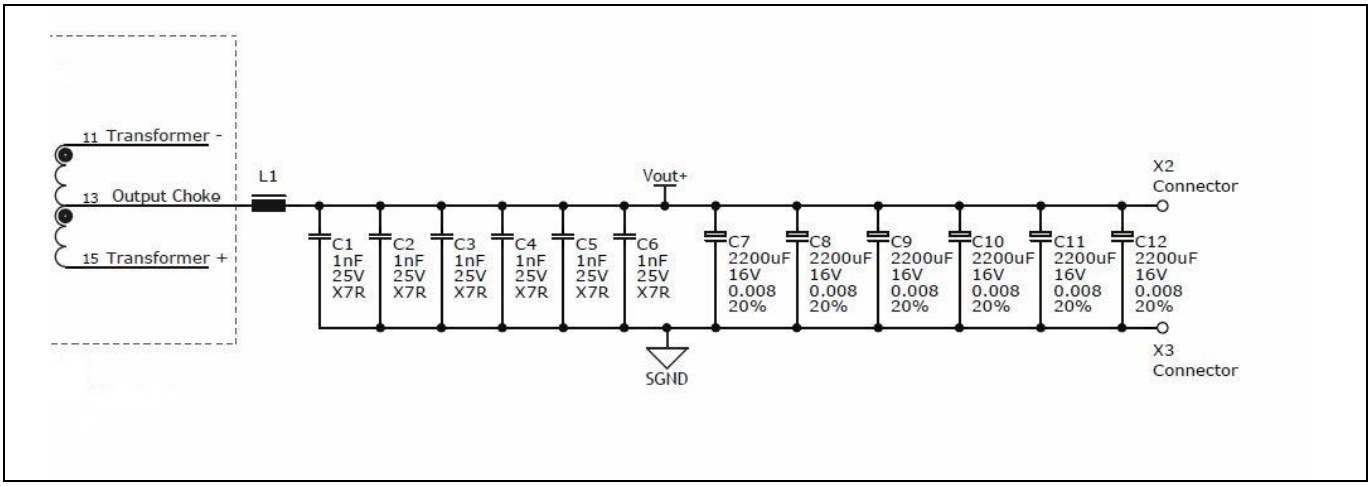


Figure 15 Secondary side

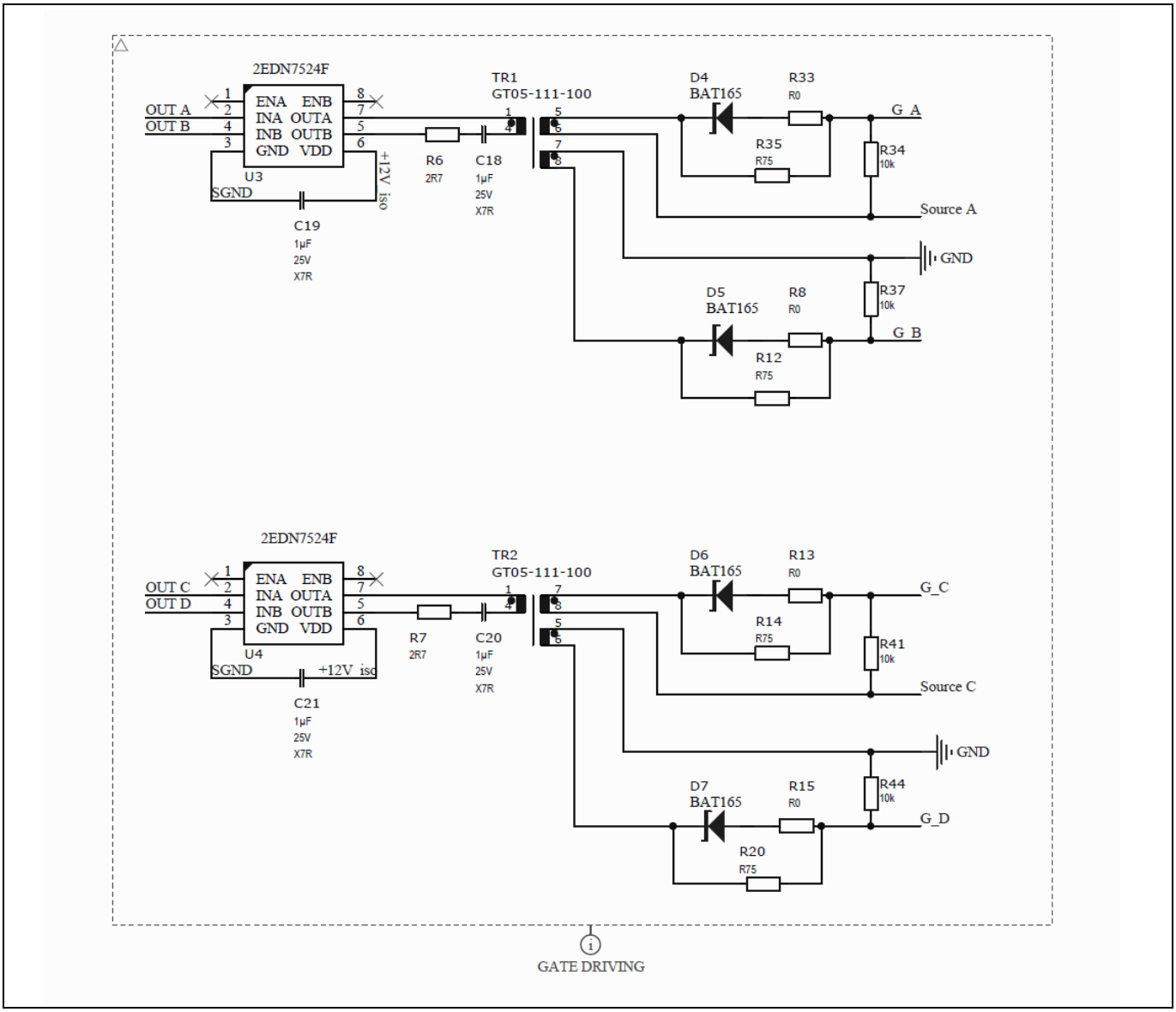


Figure 16 Gate drive

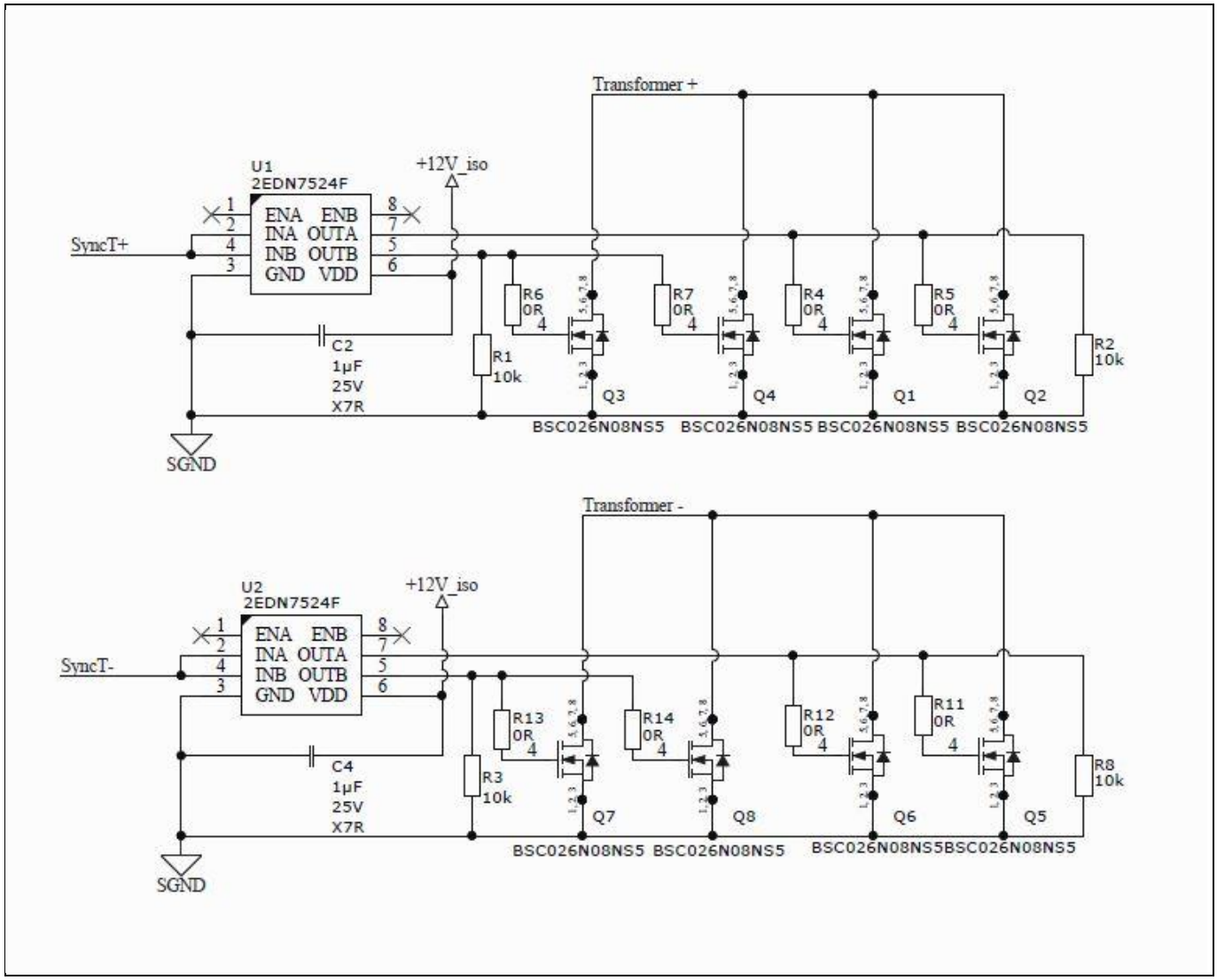


Figure 17 Synchronous rectification

3.2.2 Control board

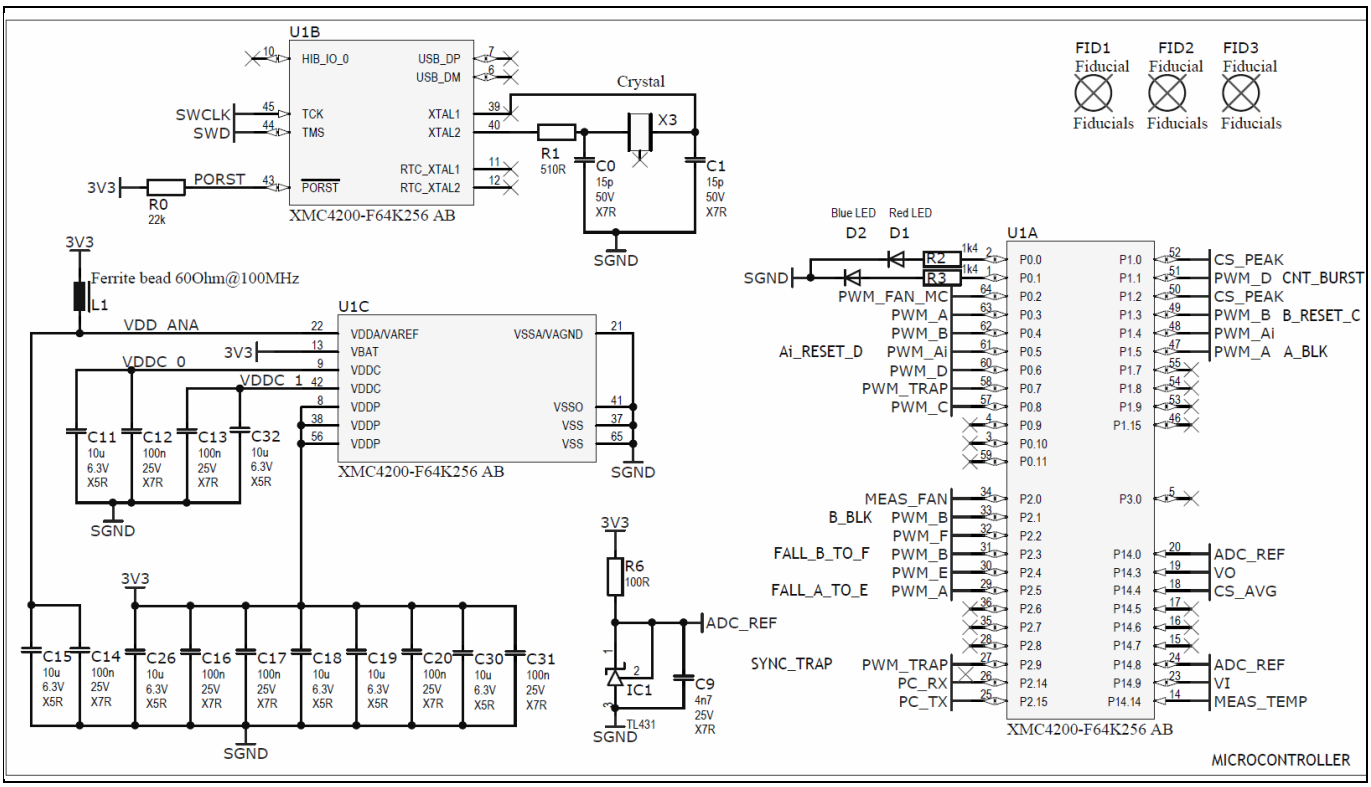


Figure 18 Microcontroller pin-out

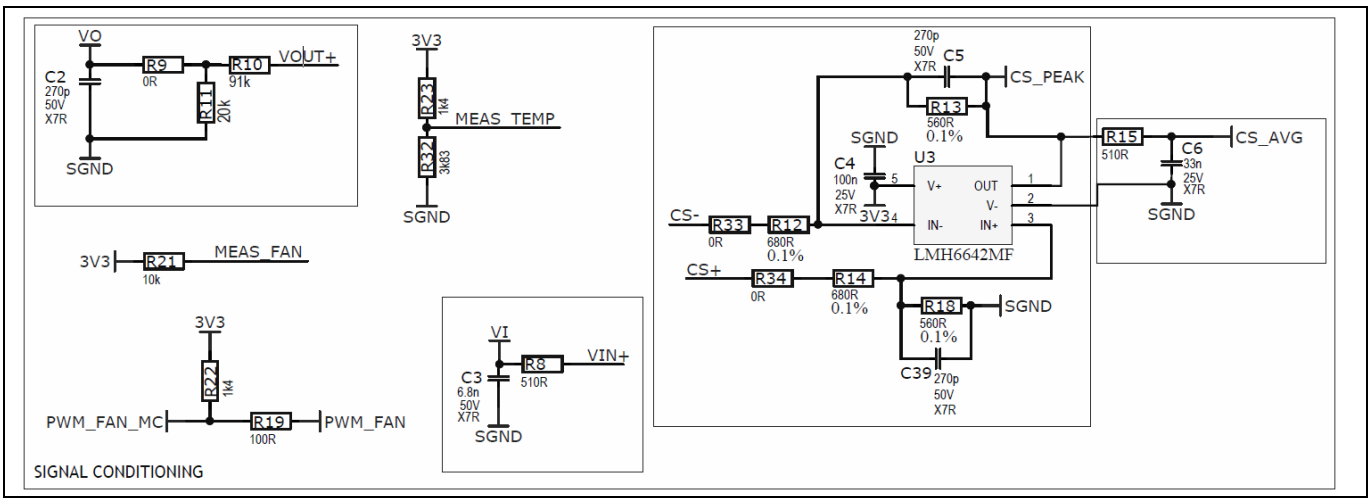


Figure 19 Signal conditioning of analog measurements (amplification and filtering)

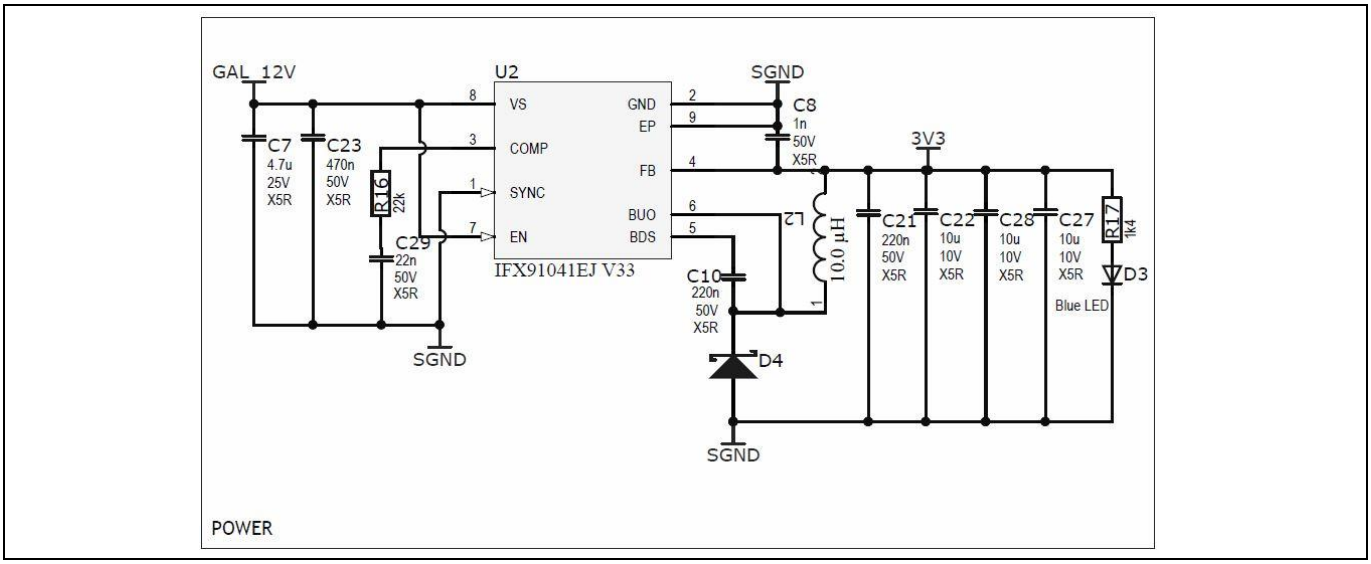


Figure 20 Supply of microcontroller and signal-conditioning circuitry

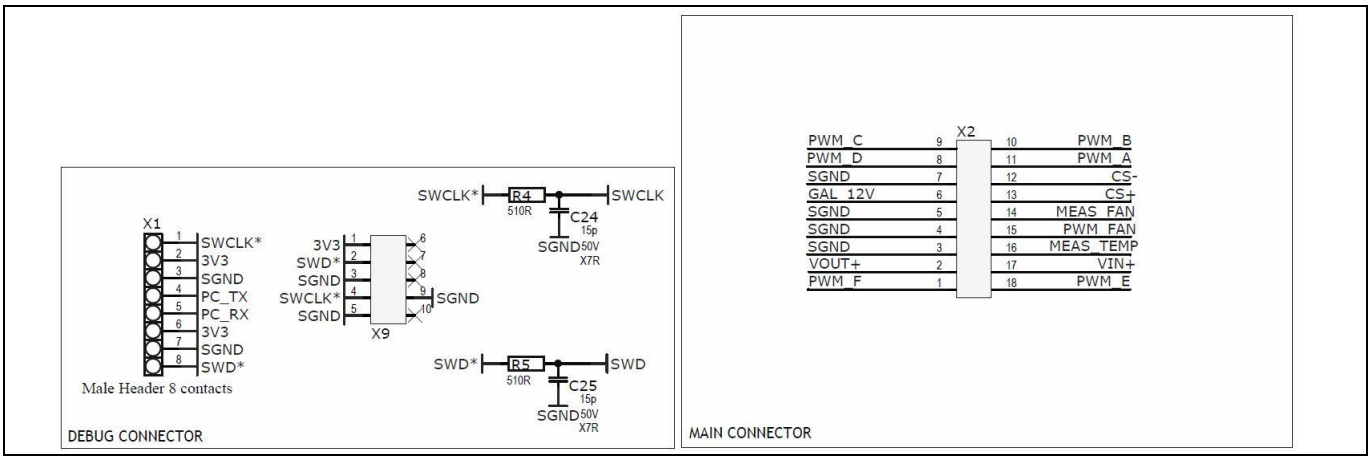


Figure 21 Control card connectors

3.2.3 Bias board (auxiliary converter)

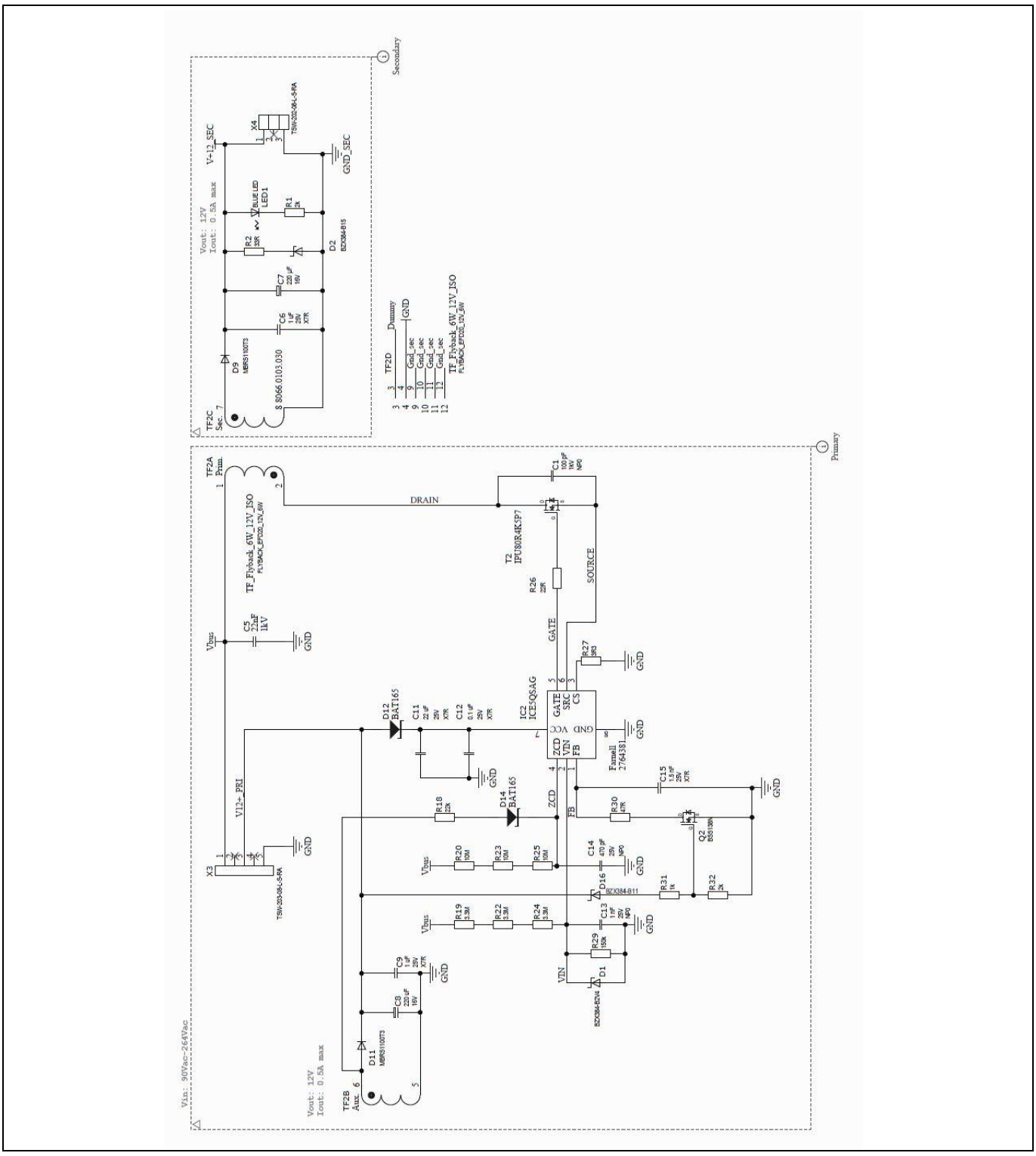


Figure 22 Bias schematic

3.3 Magnetic components

3.3.1 Main transformer

Electrical specifications at 25°C ±5°C:

Measurement	Terminal	Specification
Magnetizing inductance	2-10	2.1 mH +/-20 percent at 100 kHz, 0.5 Vrms
Leakage inductance	2-10 (11-15 shorted)	4.3 µH nominal at 100 kHz, 0.5 Vrms
Inductor inductance	1-2	12 µH +/-15 percent at 100 kHz, 0.5 Vrms
DCR	1-10 11-15	280 mΩ max. 0.6 mΩ max.
TR	2-10:11-13 2-10:13-15	22 22
Hi-pot Hi-pot Hi-pot	Pri. to sec. Pri. to core Sec. to core	4.0 kV AC, 6 mm creepage 2.5 kV AC 0.5 kV DC

Mechanical & appearance

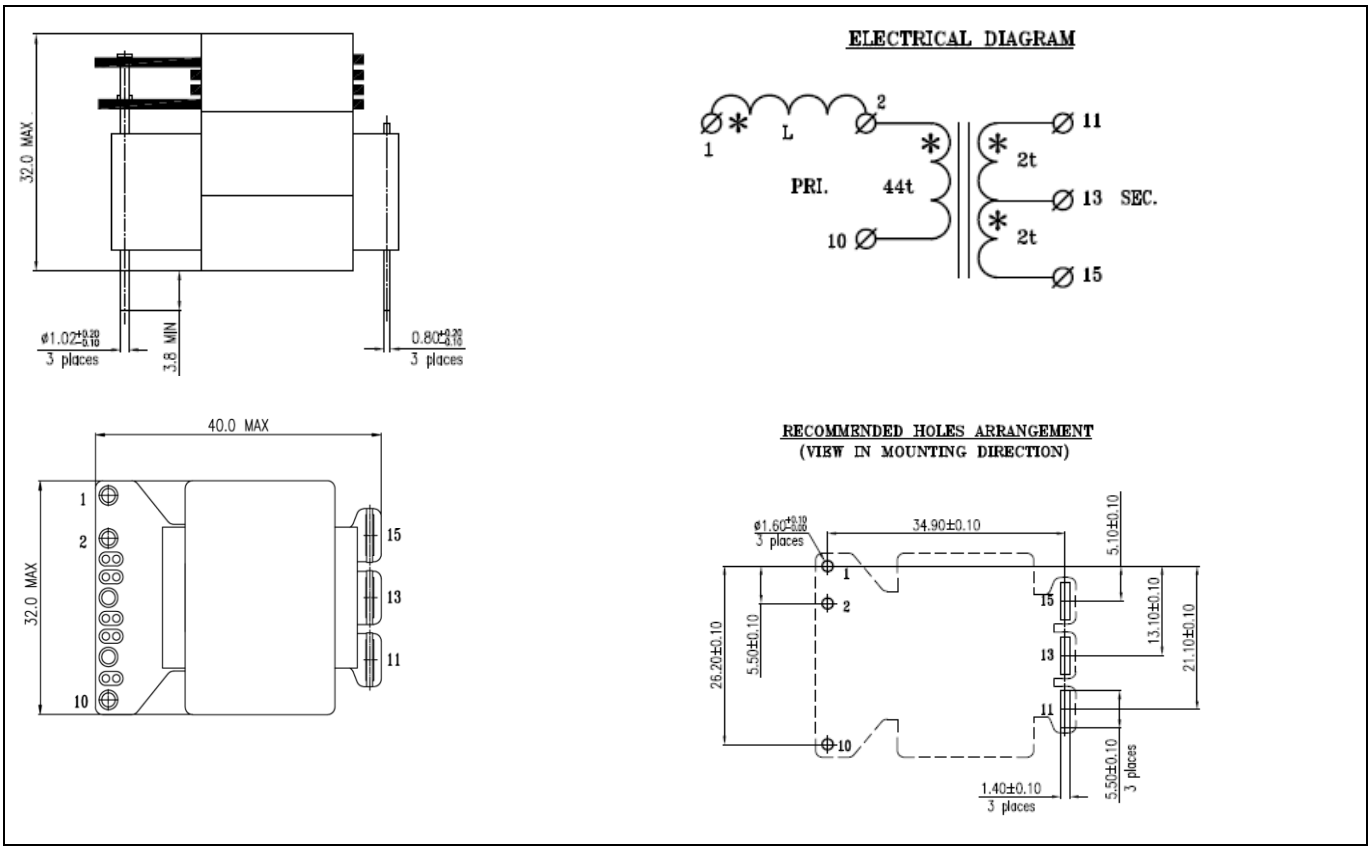


Figure 23 Mechanical and appearance – all dimensions are in mm

Module operational temperature range: -40°C up to +130°C, including module self-temperature rise.

Losses at full power (1400 W): 25 W nominal magnetic module losses.

Losses breakdown: 6 W core losses, 19 W copper losses.

23 W losses on the transformer, 2 W on the leakage inductor.

The transformer has been developed by Infineon in cooperation with the company **Payton Planar Magnetics Ltd.** – Israel – http://www.paytongroup.com/

3.3.2 Output choke



Figure 24 Output choke specification sheet

In order to take advantage of economies of scale, the same choke is used in both 800 W and 1400 W designs.

The inductor is produced by Infineon's trusted partners in the development and manufacture of magnetic components:

- **ICE Transformers s.r.l.** – Loreto Aprutino (Pescara), ITALY – http://www.icetransformers.com/en/
- **Kaschke Components GmbH** – Göttingen, GERMANY – http://www.kaschke.de/en/home/

3.3.3 Gate drive transformer

Part number	Turns ratio Drive:Gate	Drive ind. (µH, min.)	DCR (mΩ, max.)	Lkg. ind. (nH, max.)	E-T prod (V-µs)	Hi-pot Drive:Gate	Hi-pot Gate:Gate
GT05-111-100	1:1:1	2000	1430:1300	470	100	3750 V AC	1500 V DC

The gate drive transformer is a standard P/N produced by the company ICE Components, Inc.: http://www.icecomponents.com/gate-drive-transformers/

3.3.4 Auxiliary transformer

Core size	EFD20
Core material	3C95 or approved equivalent
Bobbin	Pin shine EFD20 SMT S-2005
Primary inductance	5000 µH measured from pin 1 to pin 2 at 10 kHz
Leakage inductance	Less than 50 µH measured from pin 1 to pin 2 at 10 kHz pins 5, 6, 7, 8 shorted.

*100 percent of components are hi-pot tested to 4.2 kV primary to secondary for 1 minute.

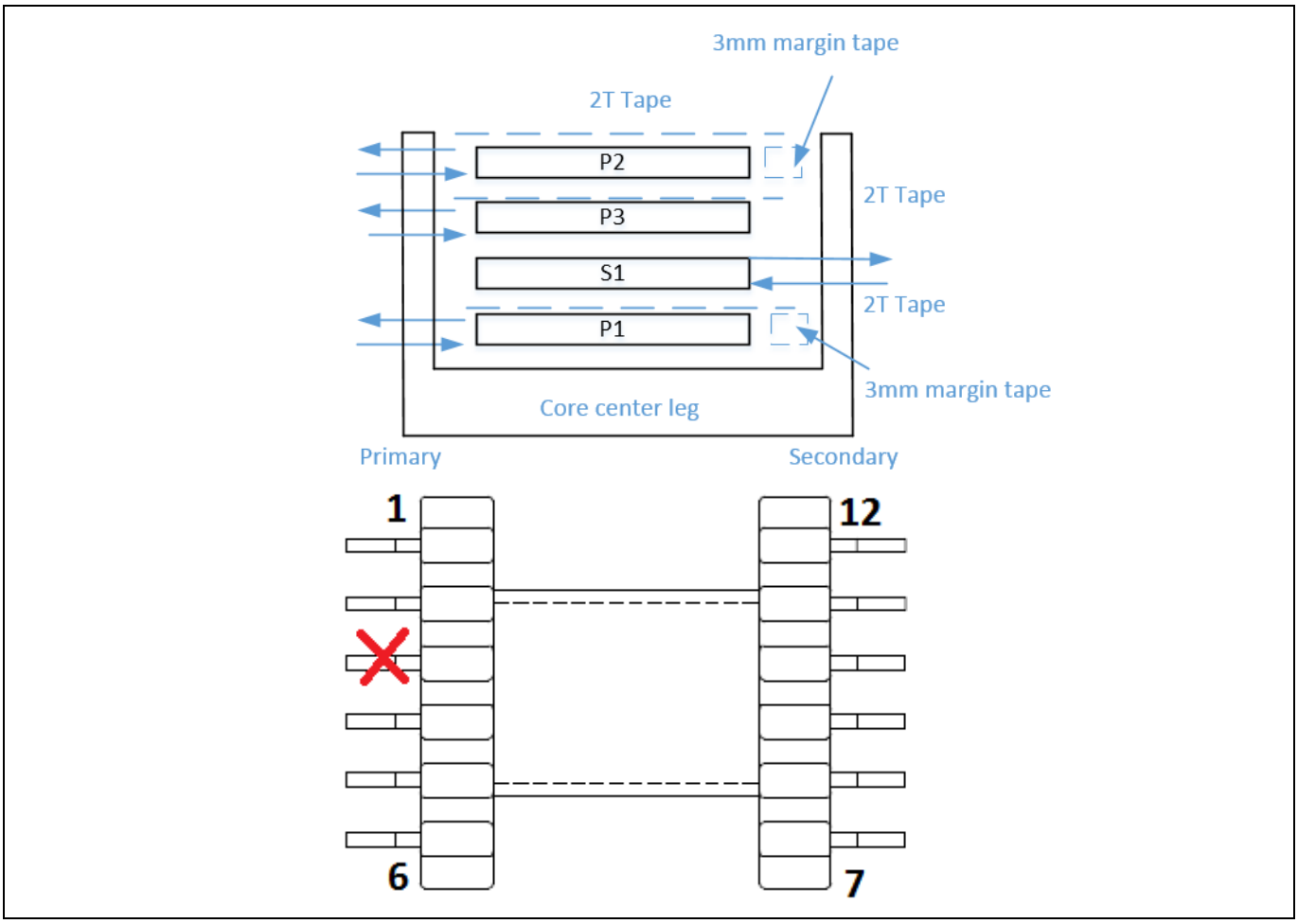


Figure 25 Flyback transformer

1. Place 3 mm of margin tape on the secondary side of the transformer (pins 7–12).
2. Place two turns of tape over the body of the entire assembly.
3. Place two turns of tape over the bottom of the transformer core or an insulator to provide creepage isolation between the pins and transformer core.
4. Clip pin 3.

Name	Start	Stop	Turns	Wire gauge	Layer	Winding
P1	2	3	65	1 × ϕ0.15 mm magnet wire	Primary	Evenly spaced
T1			2	Tape to fill window width		
S1	7	8	10	1 × ϕ 0.5 mm triple insulated	12 V_2	Evenly spaced
P3	6	5	10	1 × ϕ 0.5 mm triple insulated	12 V_1	Evenly spaced
T2			2	Tape to fill window width		
P2	3	1	65	1 × ϕ0.15 mm magnet wire	Primary	Evenly spaced
T3			2	Tape to fill window width		

The transformer is produced by Infineon's trusted partners in the development and manufacture of magnetic components:

- **ICE Transformers s.r.l.** – Loreto Aprutino (Pescara), ITALY – http://www.icetransformers.com/en/
- **Kaschke Components GmbH** – Göttingen, GERMANY – http://www.kaschke.de/en/home/

4 Digital control of PSFB

The control of the PSFB converter has been implemented using XMC4200, which is part of the XMC™ microcontroller family from Infineon Technologies. This family is based on an ARM® Cortex®-M4 core, and the main characteristics are summarized in 3.1.4. The following chapter will introduce the main features of the implemented digital control as well as the resources necessary for proper implementation.

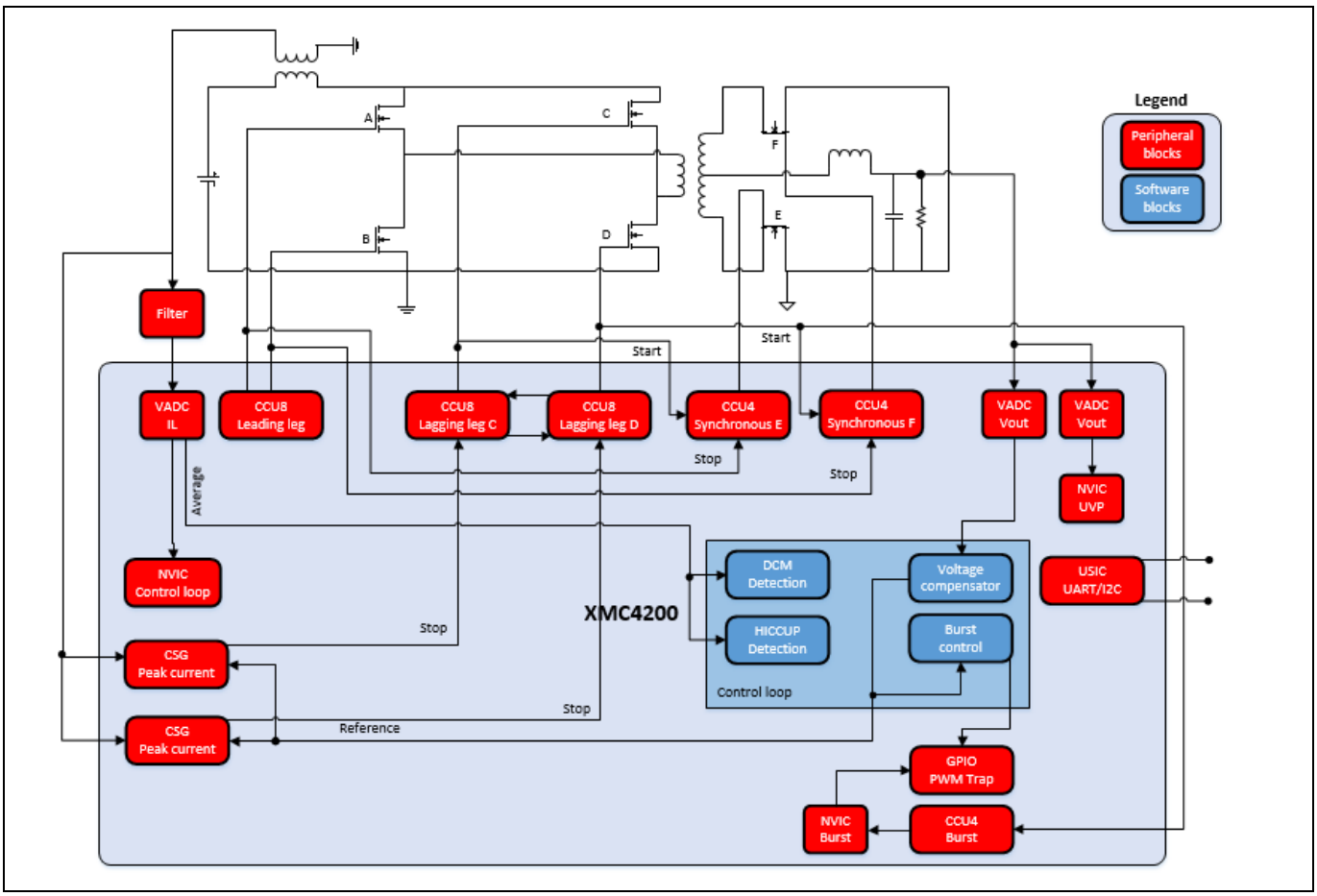


Figure 26 Simplified PCMC implementation blocks

The design, coding, documentation, testing and debugging process of digital control for the PSFB implementation with XMC4200 was supported by DAVE™ 4.1.2 and XMC™ low-level driver library (XMC™ Lib LLD).

DAVE™ 4.1.2 is a professional free-of-charge development platform for code generation provided by Infineon. Please note that XMC™ Lib and DAVE™ generated code can be used with other third-party tool chains.

There are two variants of control scheme differentiated by the PWM applied by the controller and, because of it, they have different dynamic behavior, as well as some advantages and disadvantages, which were addressed in [15].

- In Voltage Mode Control (VMC) the phase shift between the driving signals of the bridge is the control variable. The phase shift or power transfer time is proportional to the output voltage error when compared to the internal reference.
- In Peak Current Mode Control (PCMC) the peak current during a power transfer cycle is the control variable (Figure 26). The primary peak current of the transformer is proportional to the output voltage error when compared to the internal reference.

Implementation of the control with XMC4200 allows the usage of both modulation schemes without external hardware adaptations.

PCMC is recommended for this application, as the advantages over VMC enable a design with better performance in terms of efficiency and reliability.

The control routines are executed at the switching frequency (100 kHz), together with the highest-priority software protections (some of them with redundant asynchronous mechanisms). The remaining CPU time is used by the background tasks (see Figure 27).

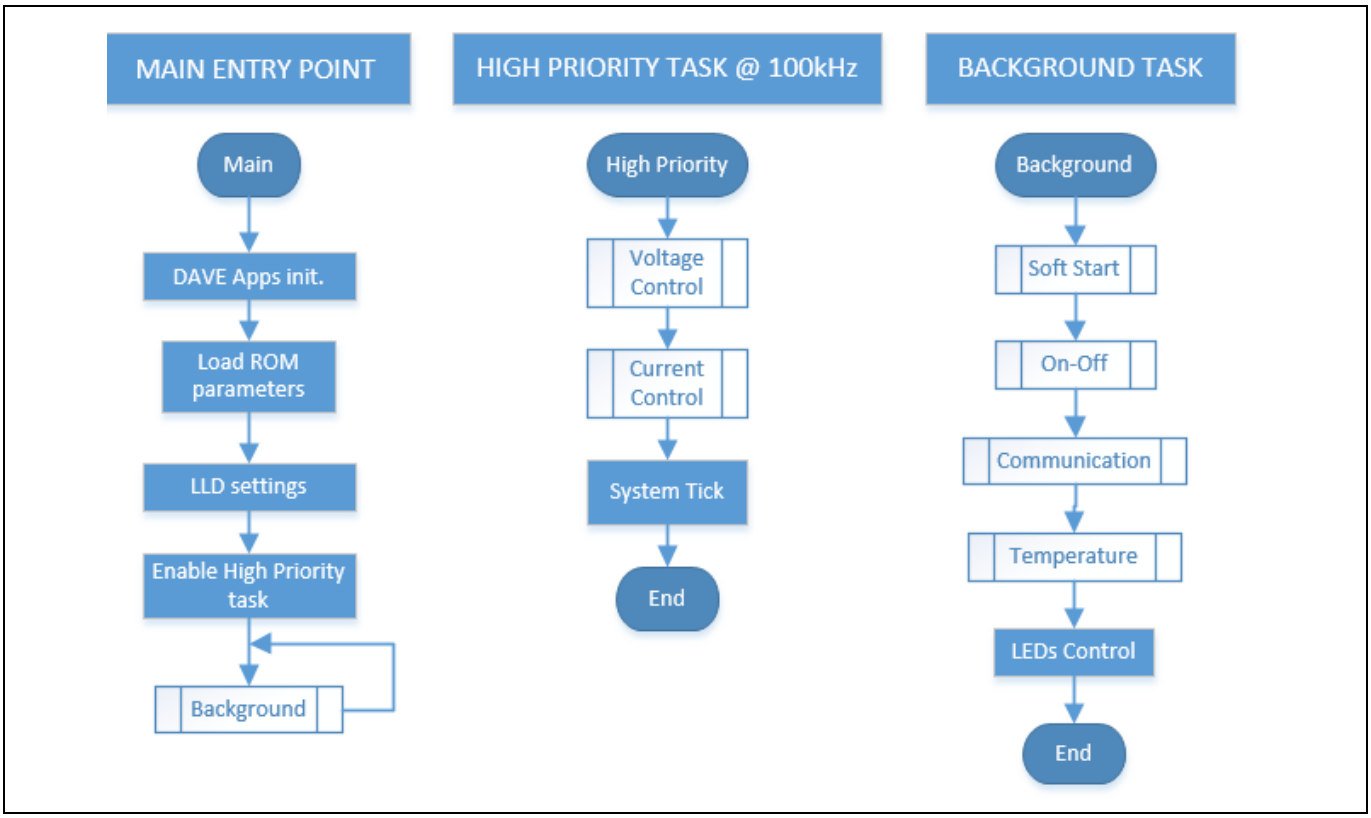


Figure 27 PSFB digital control with XMC42 main structure

Note: Hardware protections, enabled by the XMC42 peripherals, do not appear in the software flow diagrams. These redundant mechanisms provide faster reaction times to asynchronous events.

4.1 Peak Current Mode Control (PCMC)

PCMC modulation has a fixed frequency and 50 percent fixed duty for the leading leg. The lagging leg also has fixed frequency and fixed 50 percent duty cycle in steady-state. However, during transients, one or a few pulses have a different duration to adjust the phase shift between the two legs.

In PCMC the controller does not fix the timings for the pulses but the peak current to be reached during the power transfers. PWM is chopped right after reaching that value, and C or D pulses could have a shorter or longer duration to adjust the phase (Figure 28). The control delay is shorter for this modulation scheme, boosting the phase of the discrete controller.

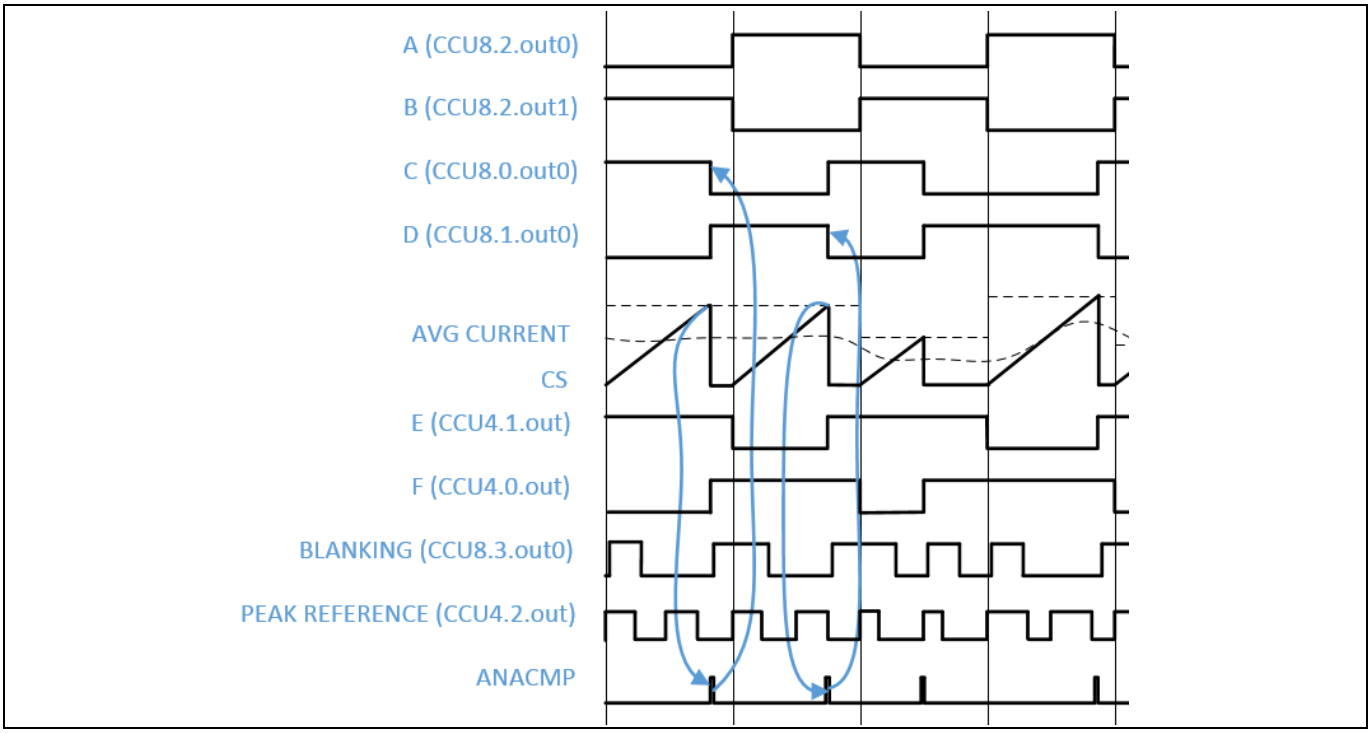


Figure 28 Current level comparison chops the PWM of the lagging leg

PCMC balances the current into the primary side of the transformer cycle-by-cycle. The phase overlap of C and D with A and B could differ, but the current will maintain its symmetry. Any potential asymmetry of the transformer excitation voltage is corrected, without the need for additional components or careful design.

Advantages of PCMC implementation with XMC4200:

- Current in the primary side of the transformer is balanced cycle-by-cycle, which avoids transformer saturation due to magnetizing current drift.
- The analog comparators included in XMC42 are equipped with DACs and slope-generation capabilities. No additional external circuitry is required. The slope compensation is required for a stable PCMC.
- There is less influence over the input voltage in the gain of the converter without additional compensation complexity.

Possible disadvantages of PCMC in the proposed implementation:

- It requires more complex control, with special consideration needed with regard to blanking times, current measurement signal conditioning and soft-start procedures.
- The DACs included in the XMC42 have up to 1023 possible levels. Resolution is limited in comparison to the VMC high-resolution steps.

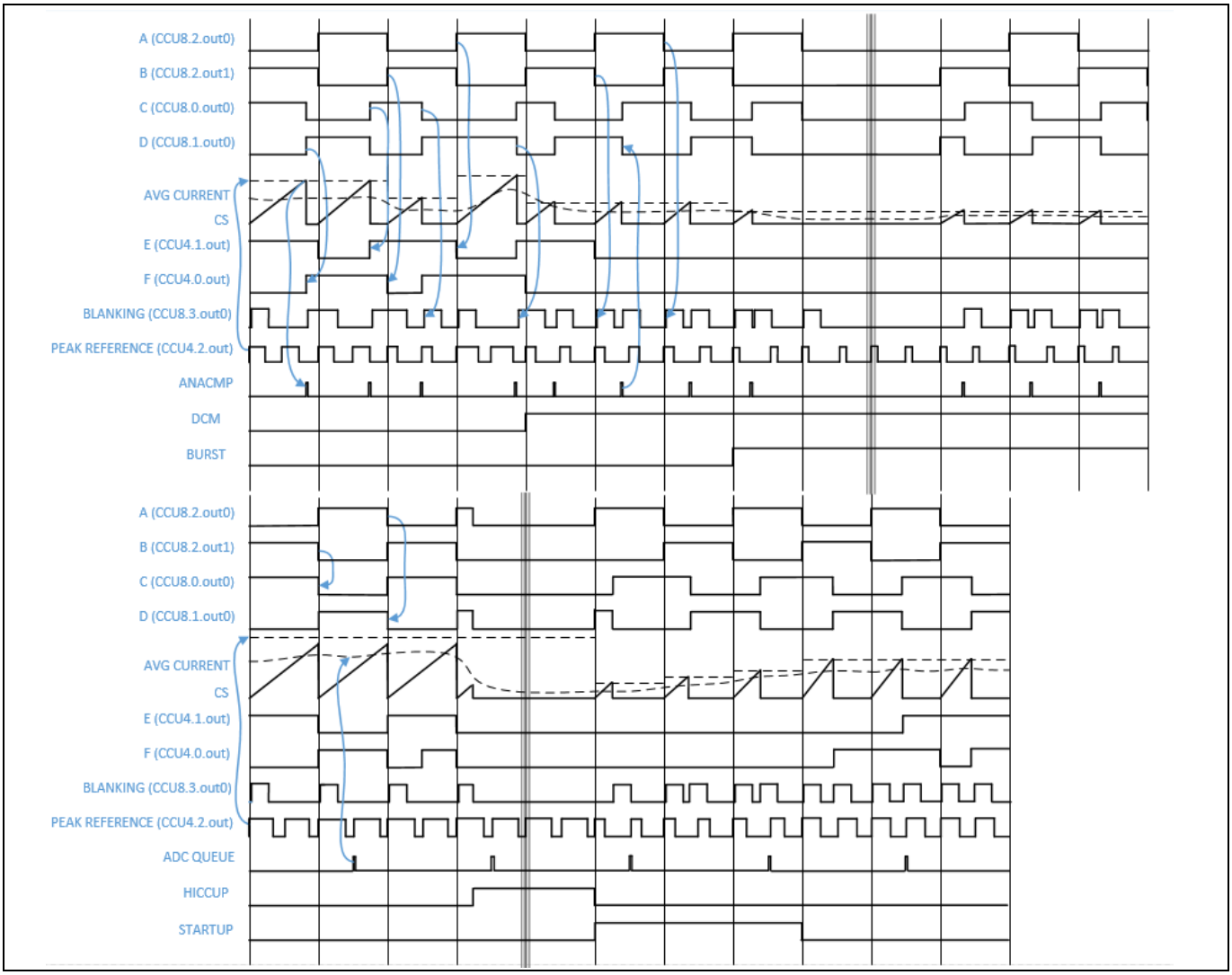


Figure 29 PCMC with XMC42

Figure 29 shows some signals and states of the controller in PCMC in more detail.

4.1.1 PCMC small-signal model

Small-signal analysis of PSFB with PCMC modulation can be found in the literature or derived elsewhere. The model here has been extracted from [9].

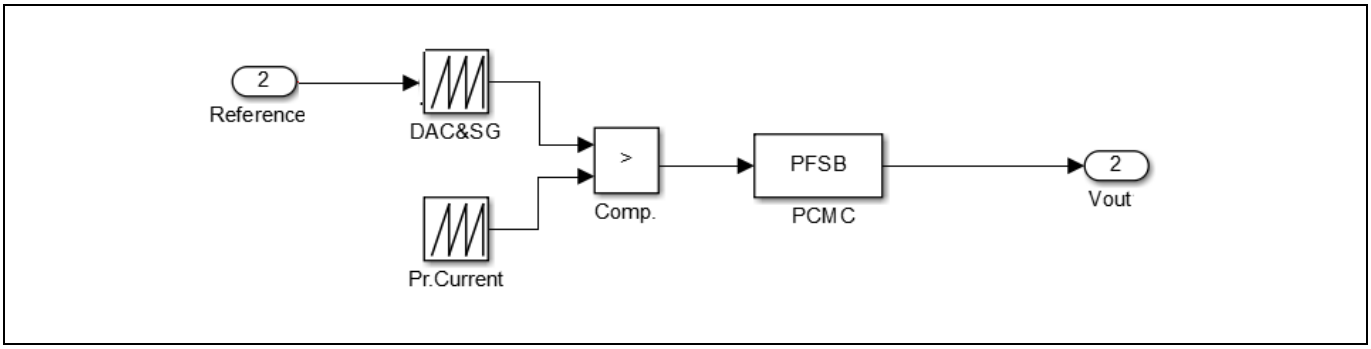


Figure 30 Modulation and converter open-loop path

The slope of the current in the primary side of the transformer including the gain of the signal conditioning is S_n. The slope compensation of the internal DAC is S_e. The gain of the modulation block for the PCMC is F_m (Figure 30).

$$M = V_{dd}/1023 \tag{7}$$

$$F_m = M * 2 * f_s/(S_n + S_e) \tag{8}$$

The gain of the CS signal path is Fi.

$$Fi = n_{sense} * R_{sense} * A_{gain} \tag{9}$$

The equivalent impedance of the output filter is Zf.

$$Zf = \frac{(Lo * Co * (Ro + Rc) * s^2 + Lo + Ro * Rc * Co * s) + Ro)}{1 + Ro * Co * s} \tag{10}$$

The equivalent impedance of the load and the output capacitor is Zc.

$$Zc = \frac{Ro + Ro * Rc * Co * s}{1 + (Ro + Rc) * Co * s} \tag{11}$$

The transformer equivalent impedance is Rd.

$$Rd = 4 * n^2 * Llkg * fs \tag{12}$$

The transfer function of the converter, reference peak current to output voltage, is Gpv.

$$F2 = n * Vin * \frac{Zc}{Zf + Rd} \tag{13}$$

$$F4 = n * \frac{Vin}{Zf + Rd} \tag{14}$$

$$F7 = 1 + \frac{Rd}{Ro} \tag{15}$$

$$F9 = n * \frac{Vin}{Ro} \tag{16}$$

$$Gpv = Fm * \frac{F2}{1 + Fm * F9 * Fi + F4 * F7 * Fm * Fi} \tag{17}$$

In PCMC the DC gain of the converter decreases at heavy loads in comparison to light loads, but has similar values for all loads in the range of frequencies where the loop would be closed, 1 kHz to 10 kHz (Figure 31).

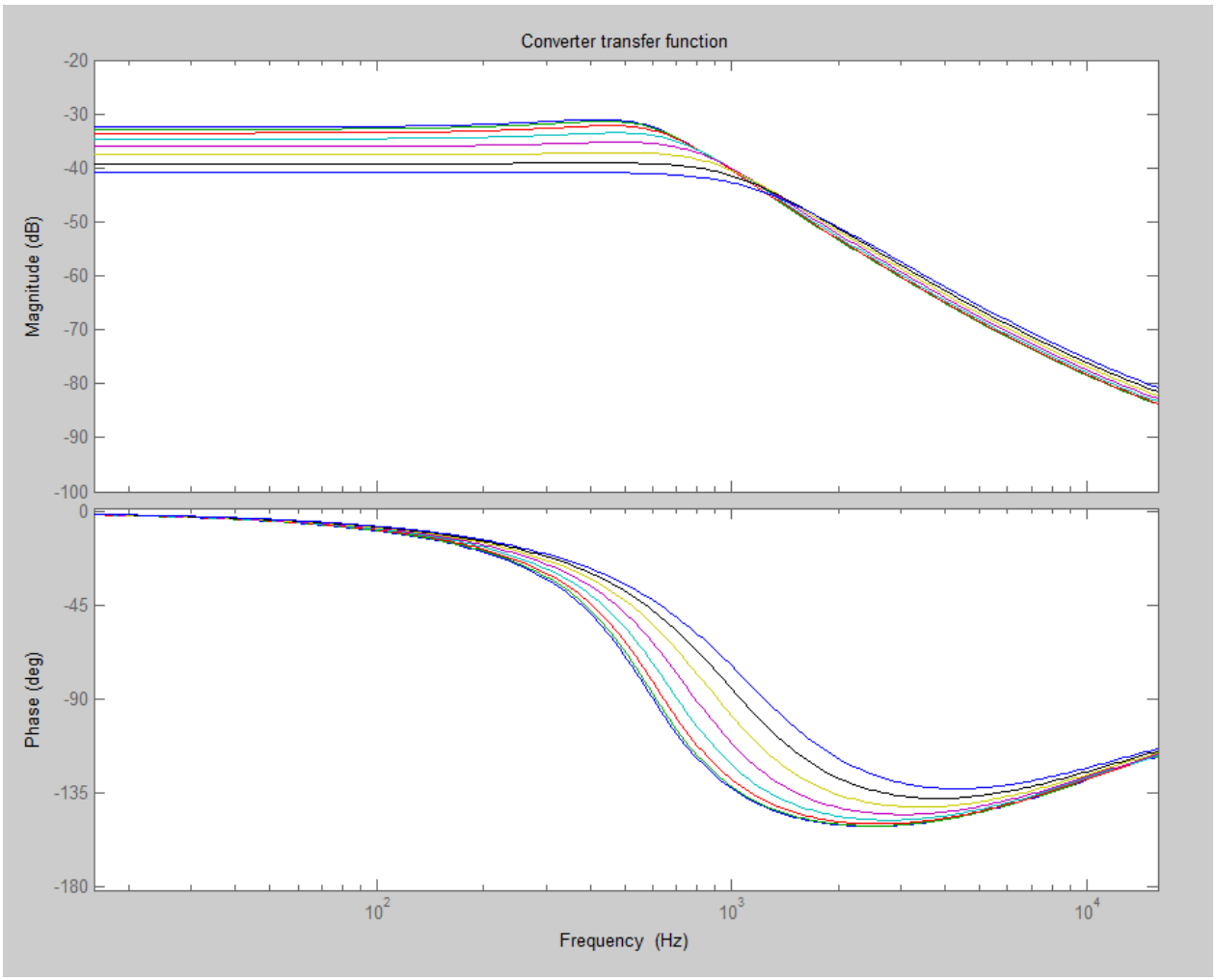


Figure 31 Open-loop frequency response of the converter, including the modulation block, for PCMC of the 1400 W PSFB

4.1.2 PCMC discrete compensator

In this mode, and for this application, there is only an outer voltage loop compensation network (Figure 32).

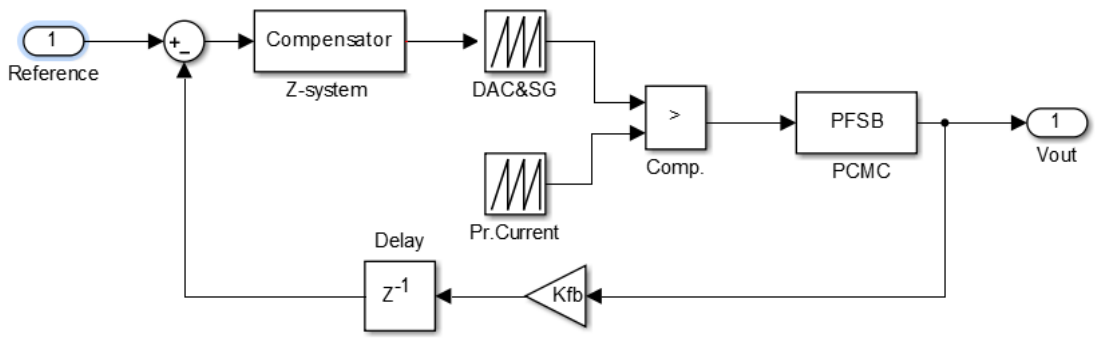


Figure 32 Compensated closed loop for PCMC

There is an inherent inner current control loop, given by the modulation scheme and stabilized by the slope compensation, which is the only control parameter to be designed in such a current loop. In the design shown,

the slope compensation is integrated using DACs available in the comparators and the slope-generation module of the XMC4200 controller. Therefore, no extra circuitry is necessary to implement this control strategy.

A two-pole and two-zero discrete compensator is designed and implemented to achieve 9.29 dB gain and 54.5 degree phase margin in the worst case scenario (Figure 33).

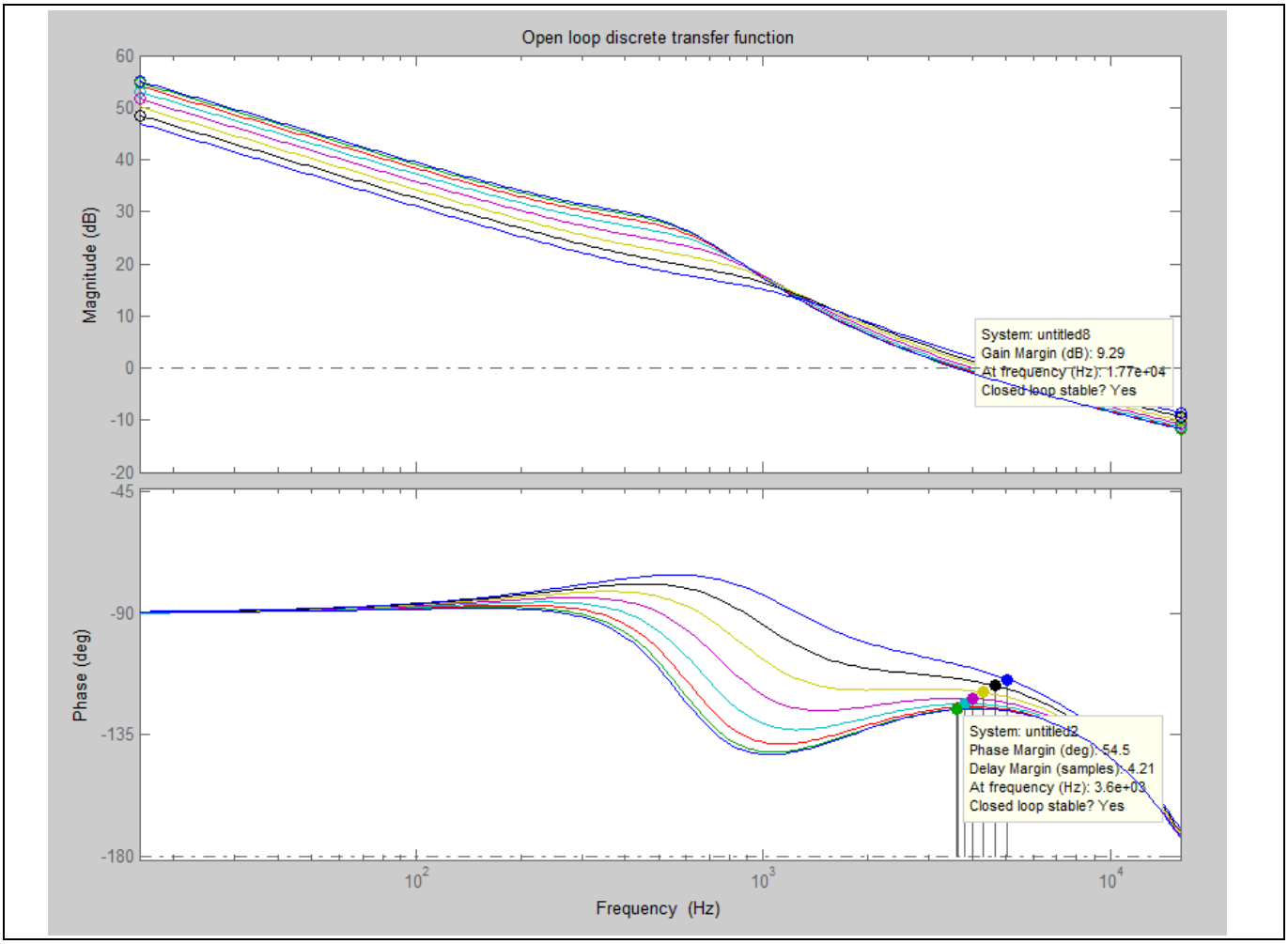


Figure 33 Loop-gain frequency response and stability margins for the designed PCMC control

4.2 Current Sense (CS)

In PCMC the CS signal path design is basic to allow for good performance of the converter.

The CS signal would ideally be scaled up to the upper supply rail of the controller (for maximum noise immunity), in this case 3.3 V. However, because of the required slope compensation (see 4.2.1) the voltage for the maximum allowed peak current should actually be lower.

The gain of the CS signal is expressed in A per V and includes the turn ratio of the CS transformer (1:100) multiplied by the gain of the CS resistors (500 Ω) and multiplied by the gain of a low pass filter on the control daughter card. For the maximum input power of the converter, plus a margin for dynamic load steps, we can estimate the maximum value of CS and adjust the gain of any of the steps to fulfill the previous slope-span condition.

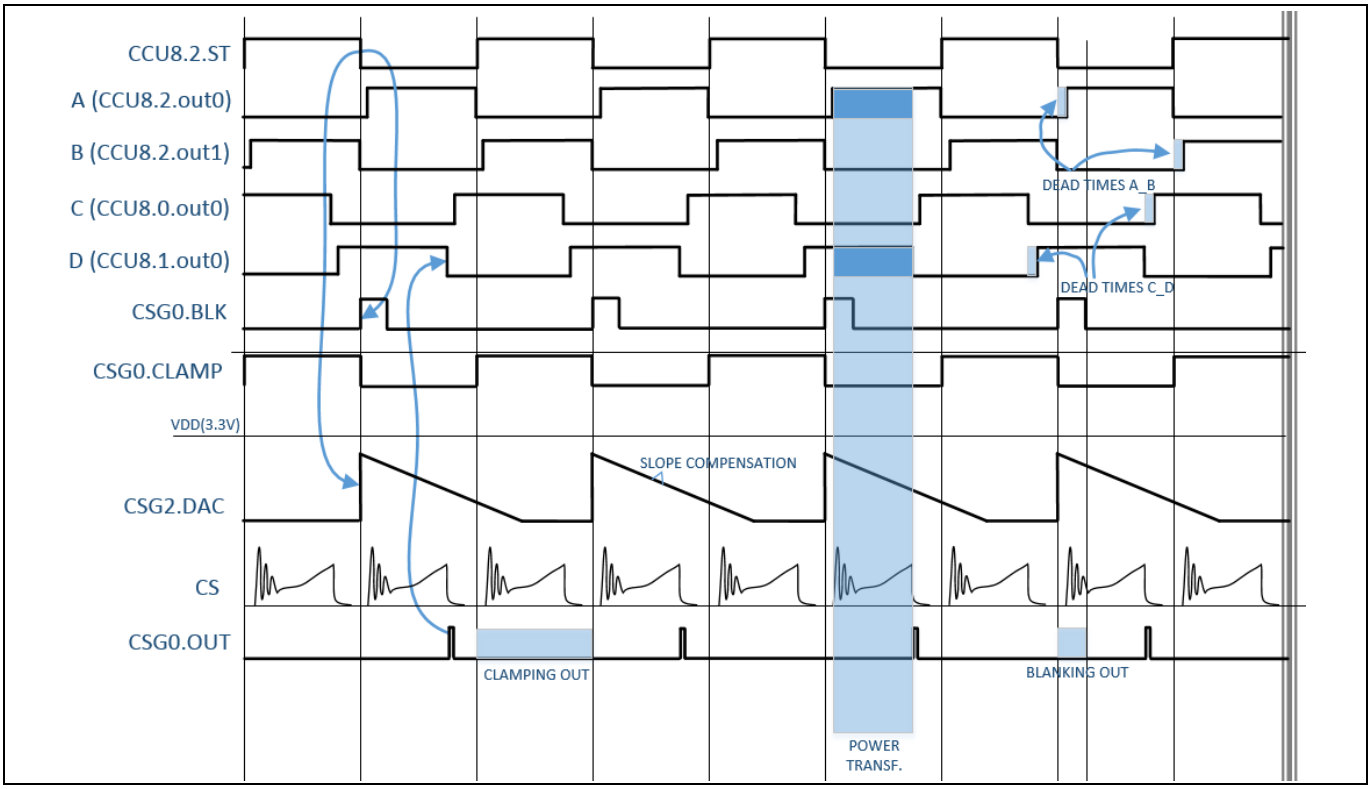


Figure 34 CSG and HRPWM simplified interconnecting events

XMC4200 provides Comparator and Slope Generator (CSG) and HRPWM peripherals with functionalities specially suited to PCMC. We take advantage of several of those mechanisms in this design (see Figure 34):

- Programmable blanking time to avoid false triggering of the comparison because of parasitic ringing of the CS at the start of the power transfer
- Configurable clamping of the output when the comparison event should be ignored, such as during power transfer of the opposite full bridge branch
- Slope compensation for damping sub-harmonic oscillations
- Independent rising and falling dead times for each timer slice that can be adjusted during run-time

4.2.1 Sub-harmonic oscillation

Sub-harmonic oscillation is an instability condition where the current through the transformer alternates between longer and shorter conduction times in steady-state (see Figure 35). In a extreme case the oscillation could lead to a transformer saturation.

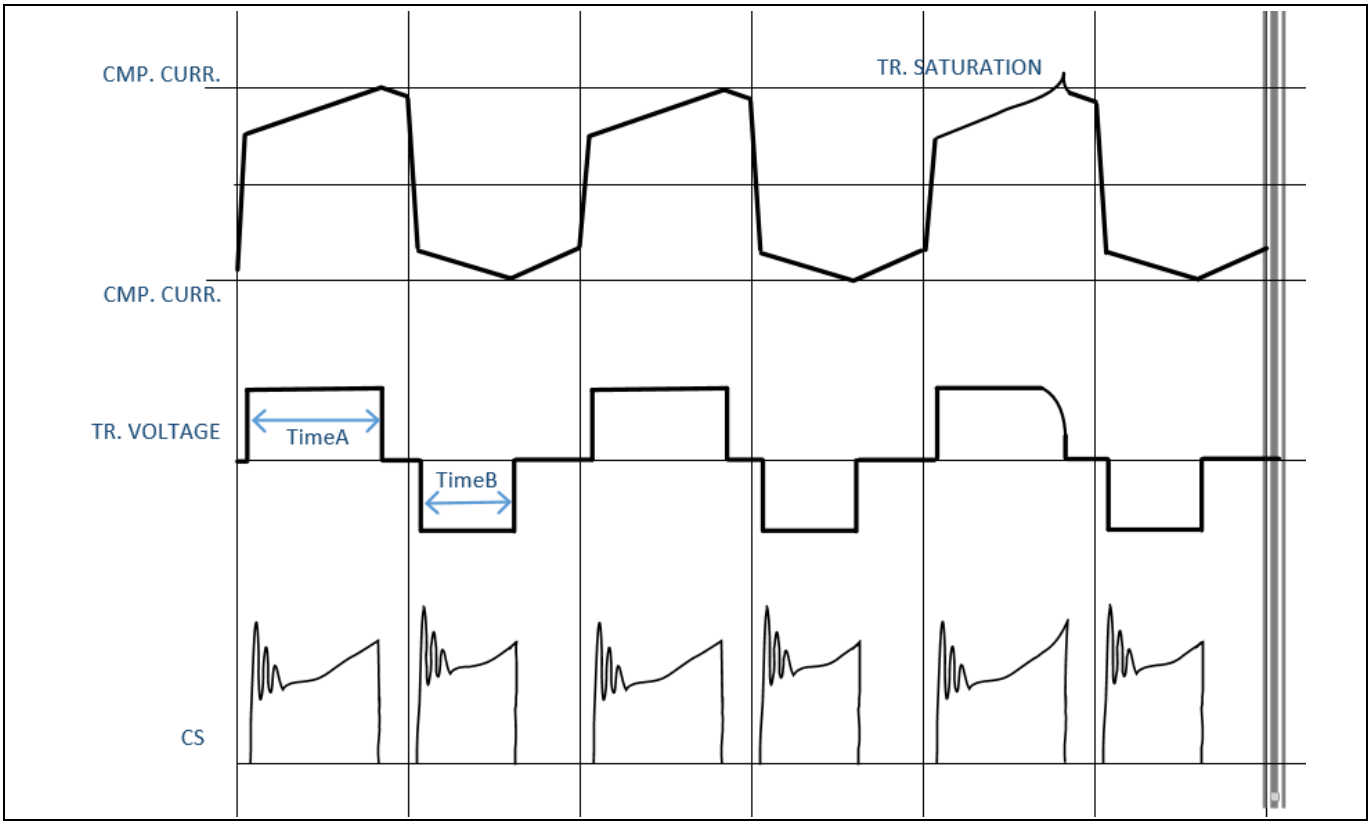


Figure 35 Sub-harmonic oscillation in PCMC PSFB

This condition could appear in PCMC whenever the duty cycle goes beyond 50 percent and there is some perturbation in the current which starts the oscillation. This oscillation will be dumped if it is ensured the rising slope of the CS is at least twice as steep as the decreasing slope.

The usual approach for increasing the rising slope of the CS is to add positive slope compensation to the CS itself or to add negative slope compensation to the comparison reference.

XMC4200 includes the CSG peripheral with integrated slope compensation without additional external components.

4.2.2 Slope generator

The CSG peripheral can generate several independent slope patterns, providing the references to the high-speed comparators. The slope can also be adjusted with fine granularity in order to achieve stability and still have room for the maximum peak current condition at full load.

The two requirements, CS span and slope compensation of sub-harmonic oscillations, are in conflict. The digital control engineer may find the best trade-off to be adjusting the CS gain and the slope value to achieve the best performance.

XMC4200's CSG makes the tuning of the slope easy and flexible.

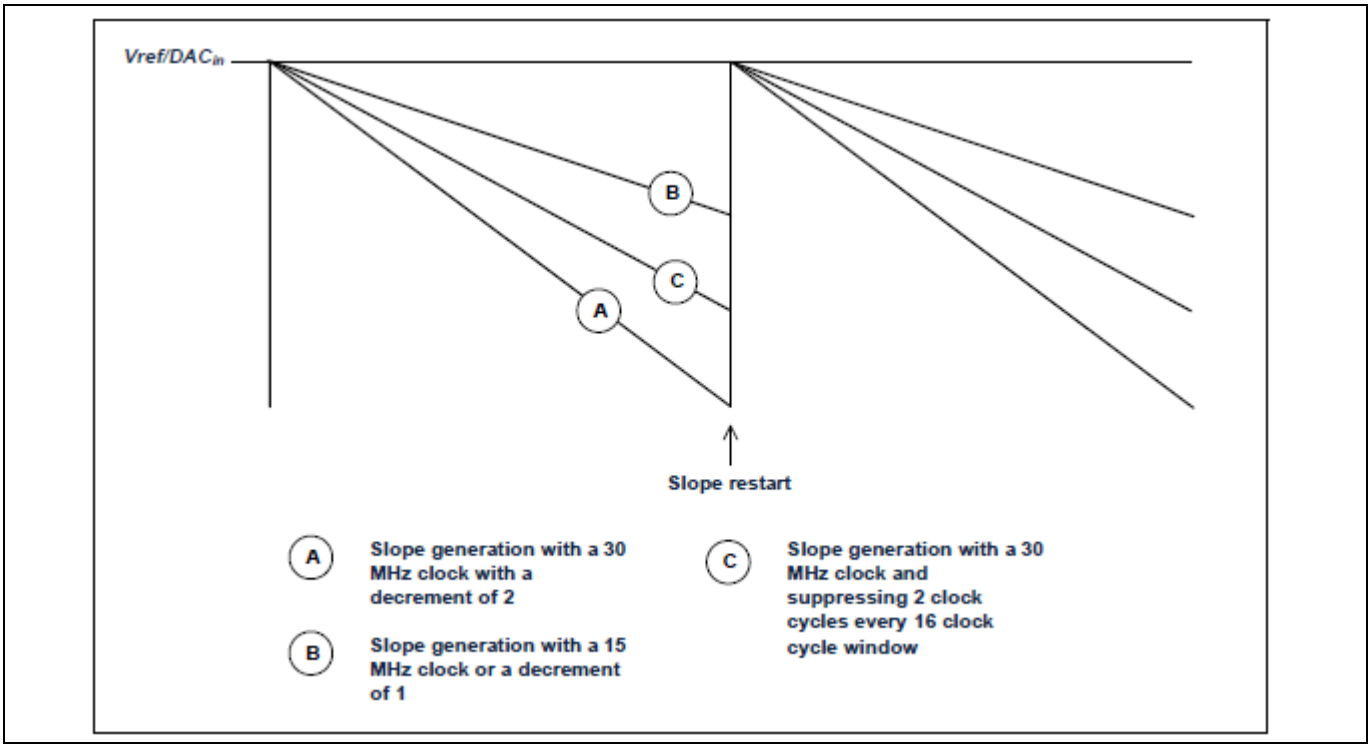


Figure 36 Example of different decrementing slopes [13].

4.3 Adaptive bridge dead times

Dead times between high-side and low-side pulses of a bridge leg may avoid shoot-through and give enough time for the output capacitance of the MOSFETs to be charged or discharged in order to achieve ZVS.

The energy available for the resonant transition changes as a function of the output load of the converter. Furthermore, the output capacitance of the HV devices is voltage dependent. As a consequence, the optimum dead times may change.

The leading leg may adapt dead times in order to always switch at the lowest point of the V_{DS} swing (valley) (Figure 37). The resonance period changes due to the non-linear output capacitance of the devices $C_{o(tr)}$.

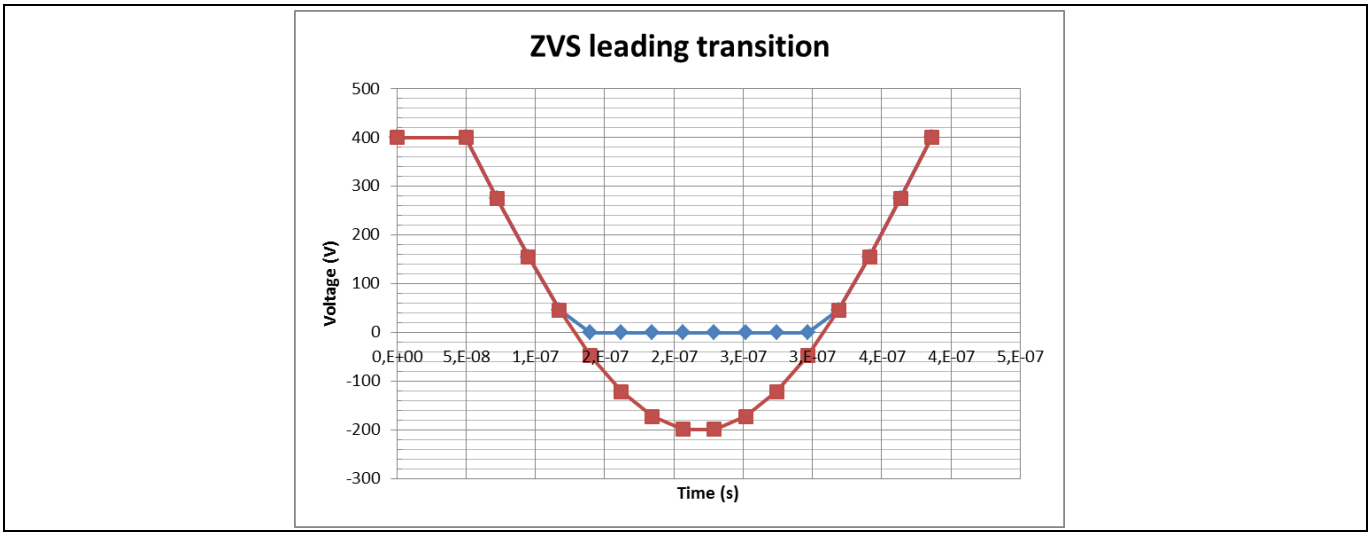


Figure 37 Leading leg resonant transition

The lagging leg may decrease the dead times for increasing loads to minimize the BD conduction and maximize the available effective duty cycle. The transition for the lagging leg is quasi-linear, but is also influenced by the non-linear output capacitance of the devices $C_{o(tr)}$ (Figure 38).

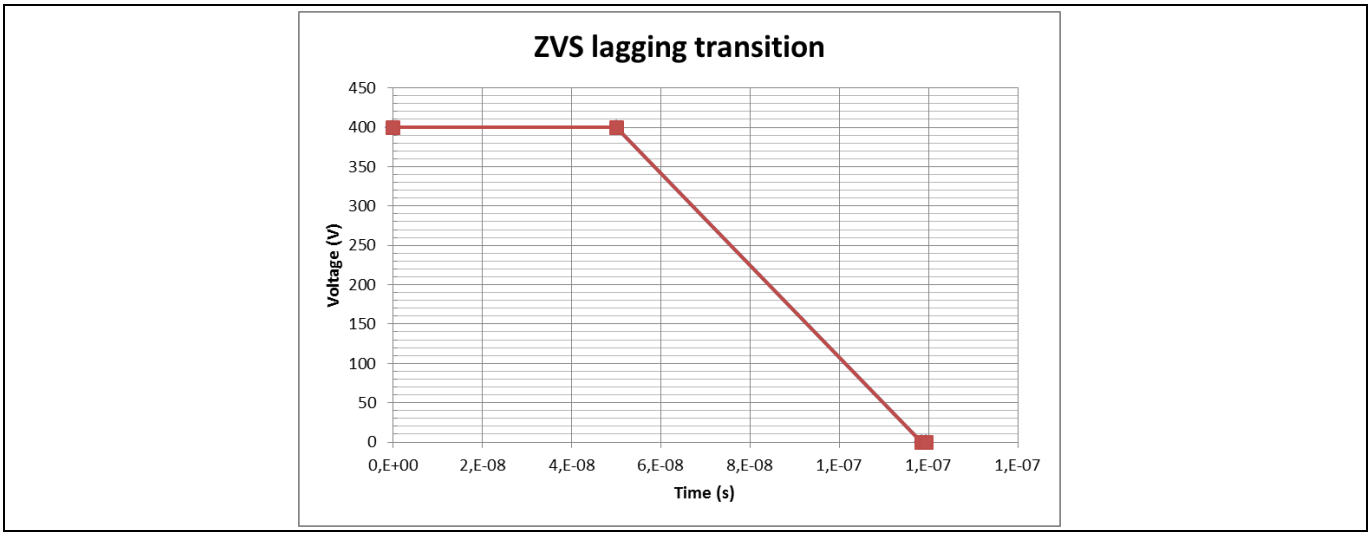


Figure 38 Lagging leg quasi-linear transition

The dependency optimum dead time to output load of the converter can be approximated by these linear formulas:

$$dtAB = dtAB_{nominal} - Io * \frac{dt_{factor}}{2^{ratio}} \quad (18)$$

$$dtCD = dtCD_{nominal} - Io * \frac{dt_{factor}}{2^{ratio}} \quad (19)$$

These formulas have little processing overhead and few parameters to adjust to reduce the optimization procedure effort (see 4.7.3).

4.4 Synchronous Rectification (SR)

The rising edge of the synchronous gate E follows the falling edge of the switch gate D. The rising edge of the synchronous gate F follows the falling edge of the switch gate C.

A dead time is required between the fall of the bridge signal and the rise of the synchronous gate. The voltage in the drain of the synchronous MOSFET is falling after the resonant transition in the primary side of the transformer. The amount of time after the fall of the bridge signal decreases as a function of the output current of the converter (see 4.2).

The voltage in the drain of MOSFET E would rise again after the falling edge of gate B (a power transfer is about to start through the opposite branch). The time after the falling edge of gate B would increase as a function of the output current due to the effect of the L_{lkg} reducing the effective duty cycle.

When the average output current is lower than the current ripple of the output filter, the synchronous conduction goes into Discontinuous Conduction Mode (DCM). Once the current becomes zero through the output choke, synchronous MOSFETS should be off to behave as pure diodes and avoid increased conduction losses due to negative current injection from the output.

There are three possible driving schemes for the synchronous rectifiers to minimize losses and overcome DCM of the output filter.

4.4.1 Synchronous MOSFETs as diodes (mode 0)

At no load or very light load, during start-up and during burst, the synchronous driving is deactivated and the BDs conduct all the current.

Under certain loads the current through the synchronous MOSFETs is low enough for the conduction losses to be equal or lower than the driving losses. At this point, it is better to stop driving the synchronous MOSFETs.

This also ensures that under DCM of the output filter there is no negative current injected back, which will only increase conduction losses and decrease performance.

4.4.2 Synchronous MOSFETs active during power transfer (mode 1)

In this mode synchronous MOSFETs are only driven during the power transfer.



Figure 39 Synchronous MOSFET gate pulse (yellow), V_{DS} (purple) and primary current of the transformer (green)

Under light load the secondary side may enter DCM. This mode avoids negative current through secondary rectifiers with lower losses than the pure diode conduction mode.

In this mode the modulation scheme of the synchronous MOSFETs changes: the rising edge of gate E is linked to the falling edge of gate A and the falling edge of gate E is linked to the falling edge of gate C, the rising edge of gate F is linked to the falling edge of gate B and the falling edge of gate E is linked to the falling edge of gate D.

4.4.3 Synchronous MOSFETs active during opposite power transfer (mode 2)

Synchronous MOSFETs are active during both the power transfer and the recirculation time, only skipping the power transfer of the opposite branch.

For maximum efficiency, the driving of the synchronous MOSFETs should minimize BD conduction but should maintain enough margins not to overlap voltage in the drain (V_{DS}) and voltage in the gate (V_{GS}).

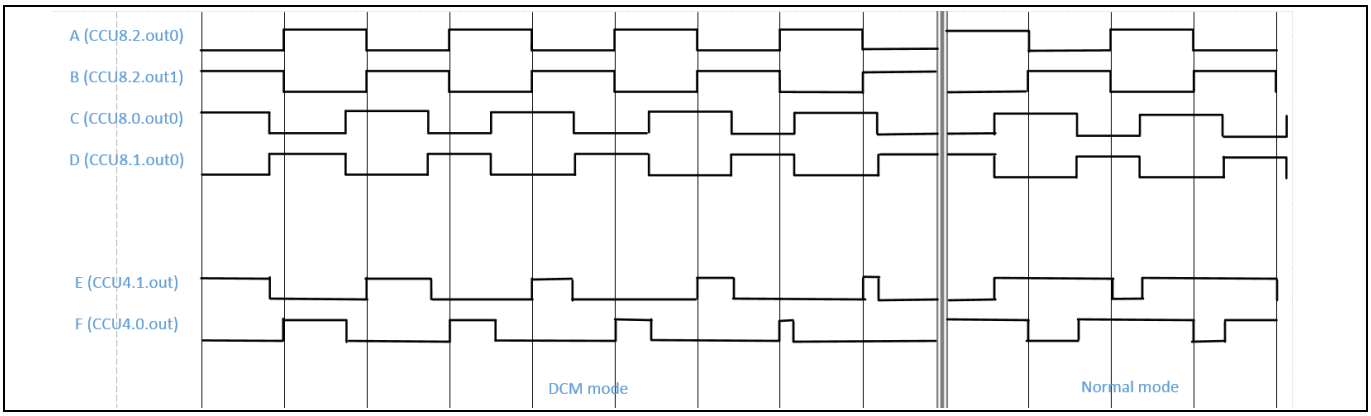


Figure 40 Synchronous MOSFETs modulation schemes: modes 1 and 2

4.4.4 Adaptive synchronous conduction time

For increasing output currents, the effective duty cycle is reduced. The margin V_{GS} to V_{DS} of the synchronous MOSFETs also increases due to the finite time for the resonant inductance current reversion.

A dynamic adjustment of the conduction times of the synchronous MOSFETs, displacing both the rising and falling edges, minimizes the BD conduction time. The nominal turn-on and nominal turn-off are indicated by the vertical blue lines in Figure 41. The introduced delays are represented by the shaded blue boxes.

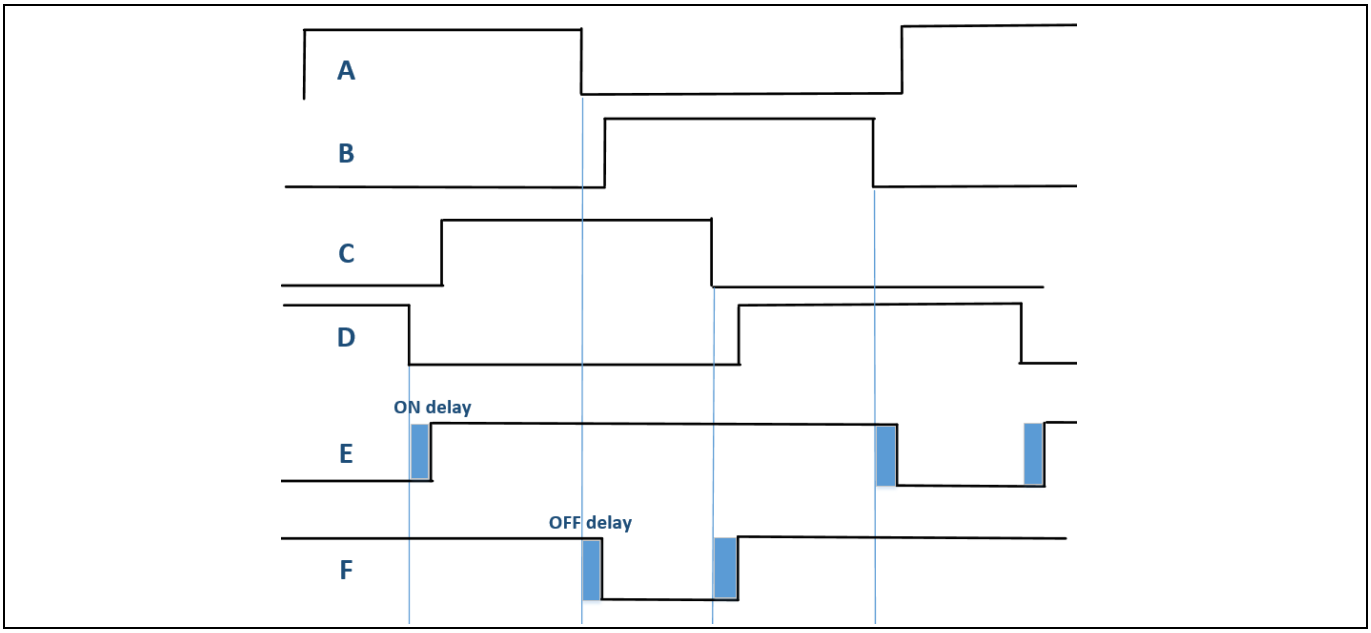


Figure 41 Adaptive delay in the turn-on and the turn-off of the synchronous MOSFETs

A linear function is applied to move the rising and falling edges, based on the average transformer primary current:

$$dtON = dtON_{nominal} - Ipr * \frac{dt_{ONfactor}}{2^{ONratio}} \quad (20)$$

$$dtOFF = dtOFF_{nominal} - Ipr * \frac{dt_{OFFfactor}}{2^{OFFratio}} \quad (21)$$

The parameters for those functions can be set through the GUI and stored in the internal memory of the controller.

4.5 Burst mode

At light load burst mode is used to further decrease losses at the expense of higher output voltage ripple (Figure 42).



Figure 42 Burst ripple: output voltage (green), primary current (yellow), V_{GS} of bridge low-side MOSFET (purple) and V_{DS} of bridge low-side MOSFET (blue)

4.5.1 Maximum-frequency limited burst

A fixed number of pulses are applied to the bridge ($BURST_{LENGTH}$). An even number of pulses is preferred, to maintain the transformer excitation voltage symmetry. Bursts of pulses always start at the same gate signal, also to avoid excitation asymmetries.

The amount of time until the next burst starts ($BURST_{TRAP}$) can be configured. In this way there is a fixed relation between the number of pulses and the time between bursts that determines the maximum frequency of the burst.

$$F_{BURSTmax} = \frac{BURST_{TRAP}}{BURST_{TRAP} + BURST_{LENGHT}} * CTRL_{frq} \quad (22)$$

$$CTRL_{frq} = 100kHz \quad (23)$$

The minimum frequency varies depending on the load conditions. A hysteresis window delimits a non-switching, a burst mode and a normal switching range (Figure 44) as a function of the compensation network output.

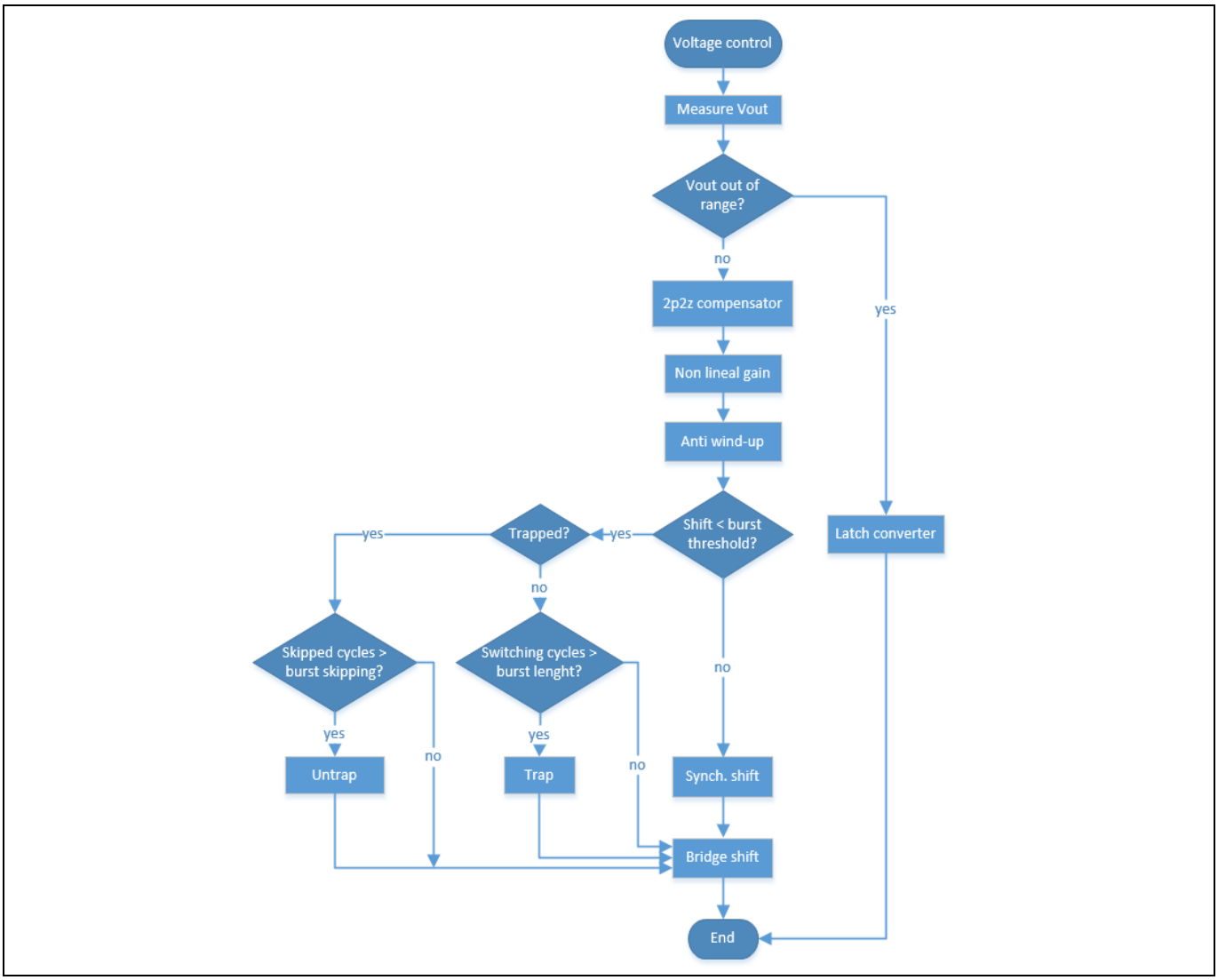


Figure 43 Regulation and burst control flow diagram

The parameters influencing burst algorithm (Figure 43) behavior are:

- Burst stop: lower limit of the hysteresis window delimiting the non-switching and the burst mode ranges (see Figure 44)
- Burst low threshold: lower limit of the hysteresis window delimiting the burst mode and the normal mode ranges
- Burst high threshold: upper limit of the hysteresis window delimiting the burst mode and the normal mode ranges
- Minimum phase: minimum phase shift applied to the gate signals during normal mode
- Burst phase: minimum phase shift applied during burst mode; setting high values may increase burst ripple but improve efficiency

- Burst skipping cycles: number of switching cycles skipped after a burst ($BURST_{TRAP}$ in equation 22)
- Burst length: number of pulses applied during a burst ($BURST_{LENGTH}$ in equation 22)

These parameters can be adjusted using the GUI and stored in the internal memory of the microcontroller.

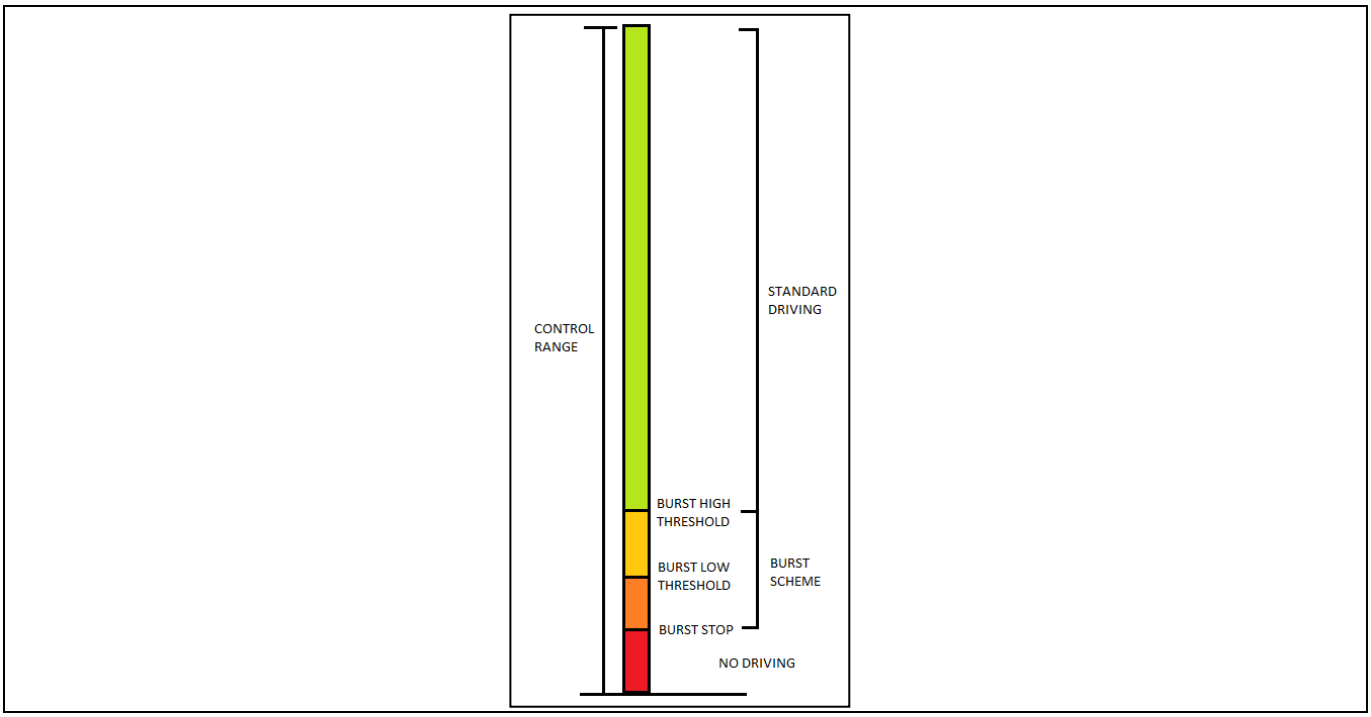


Figure 44 Burst mode thresholds based on the compensator output

4.6 Protections

4.6.1 Over Current Protection (OCP)

There are several redundant mechanisms for OCP of the converter, described in detail in the following sections.

4.6.1.1 Cycle-by-cycle OCP

In PCMC there is an inherent cycle-by-cycle Peak Current Limitation (PCL) of the primary current (Figure 45).

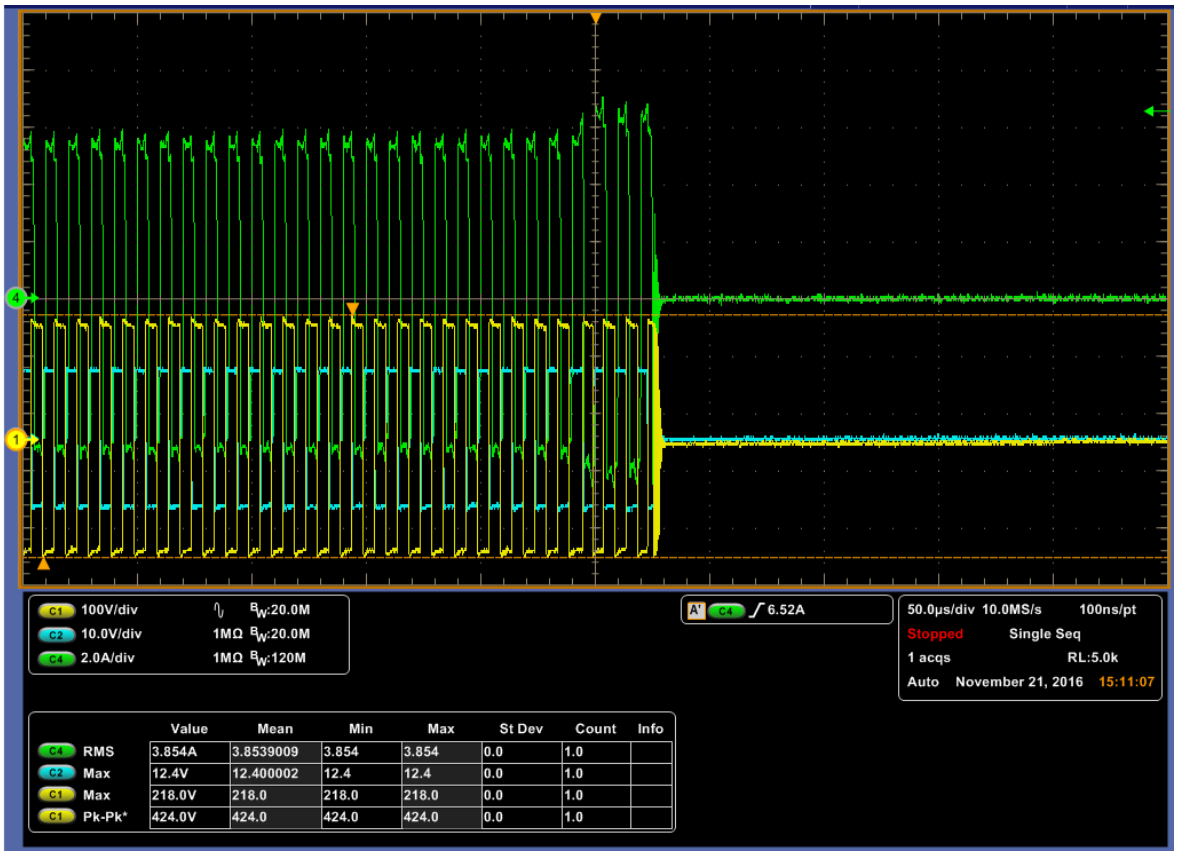


Figure 45 Cycle-by-cycle limitation in an output short-circuit event: primary current (green), V_{GS} of bridge low-side (blue) and V_{DS} of bridge low-side MOSFET (yellow)

4.6.1.2 Output OCP

There is no direct output current measurement in the PSFB 800 W design. Output current is calculated as a function of the input current and the input voltage. The same input current is proportionally higher output current for higher input voltages.

This is the formula applied for the scaling of the OCP not requiring direct measurement of the output current:

$$I_{limit} = I_{limit_nominal} - (Vin - Vin_{min}) * HICCUP_{factor}/2^{HICCUP_{ratio}} \quad (24)$$

$HICCUP_{factor}$ and $HICCUP_{ratio}$ approximate the output current proportional dependency with the input voltage. These parameters are hard-coded into the firmware of the converter.

After a prolonged OC event the converter will enter hiccup mode. It will stop and try to restart after a pause (Figure 46). The converter will operate normally after the over-load resumes.

In the event of a severe output over-load, the start-up sequence will be cancelled and the converter latched up.

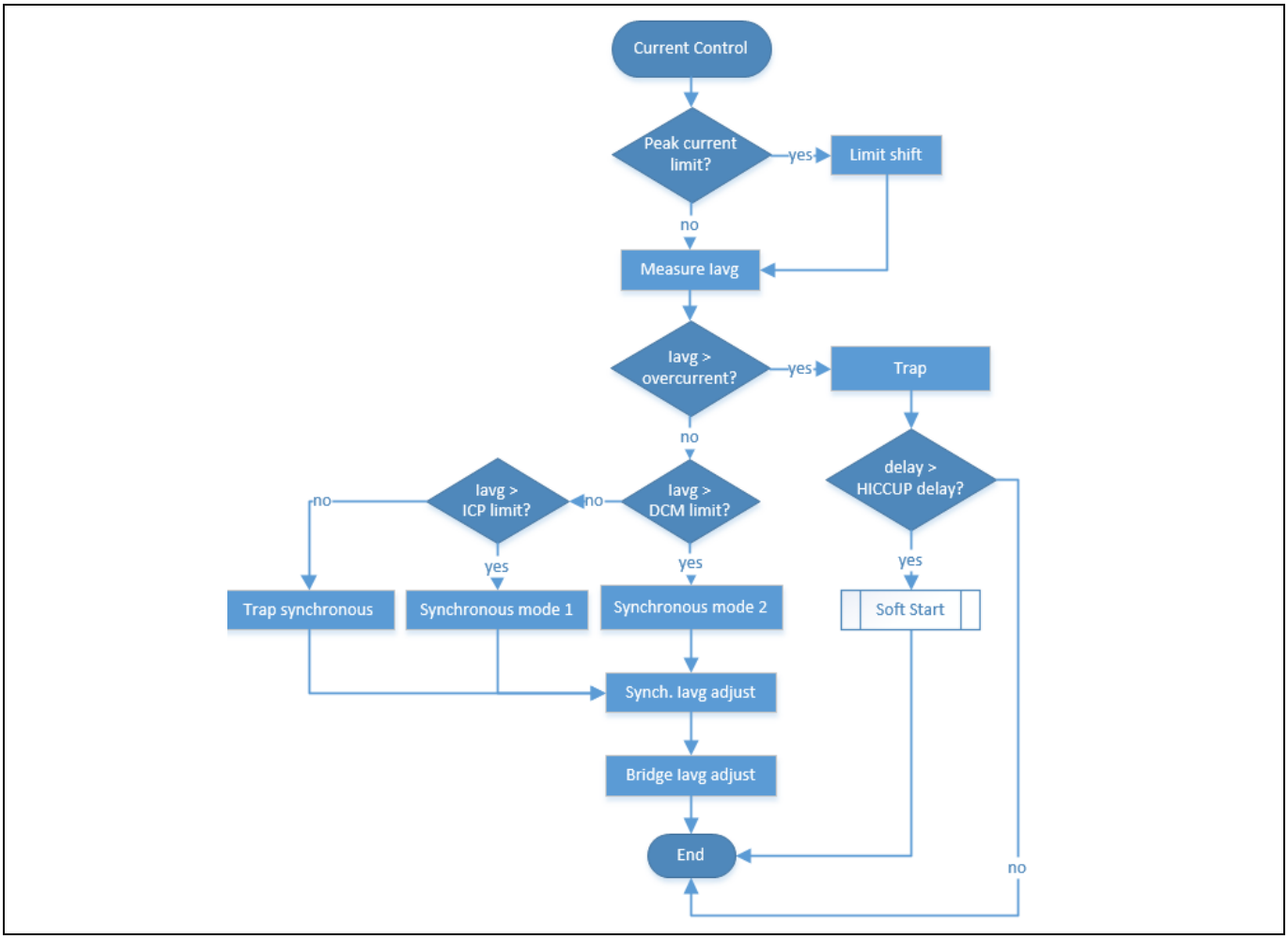


Figure 46 Output OC detection flow diagram

4.6.2 Input Under Voltage/Over Voltage Lockout (UVLO-OVLO)

The converter PSFB 800 W is designed to operate at a certain input voltage range. Input Under Voltage Lockout/Over Voltage Lockout (UVLO-OVLO), hereafter referred to as brown-in and brown-out protection, ensures that the converter does not work outside of those conditions, in order to protect the system and the devices from excessive stress outside of the specifications.

There is a hysteresis window for the brown-in and brown-out thresholds. The converter starts running above 350 V and stops again whenever the input voltage decreases to 340 V.

Above 420 V input the converter stops and will start again if the input voltage decreases to 400 V.

An isolated amplifier is used for the measurement of the input voltage from the secondary side. The isolated amplifier has a deviation in the gain between samples, and due to this, the levels should be cut.

Only the 350 V level has to be parametrized. The rest of the levels are calculated by the controller as an offset from the 350 V point. The parameter can be adjusted using the GUI provided (Figure 56).

4.6.3 On-off control

If the converter is connected to the user interface there is the option of remote start and stop. The on-off mechanism precedes the brown-in-out (see Figure 47).

Note: Brown-in and brown-out mechanisms prevail over the remote start and stop command. Only under the specified operating range can the converter be started – unless the brown-in-out protection is deactivated from the GUI.

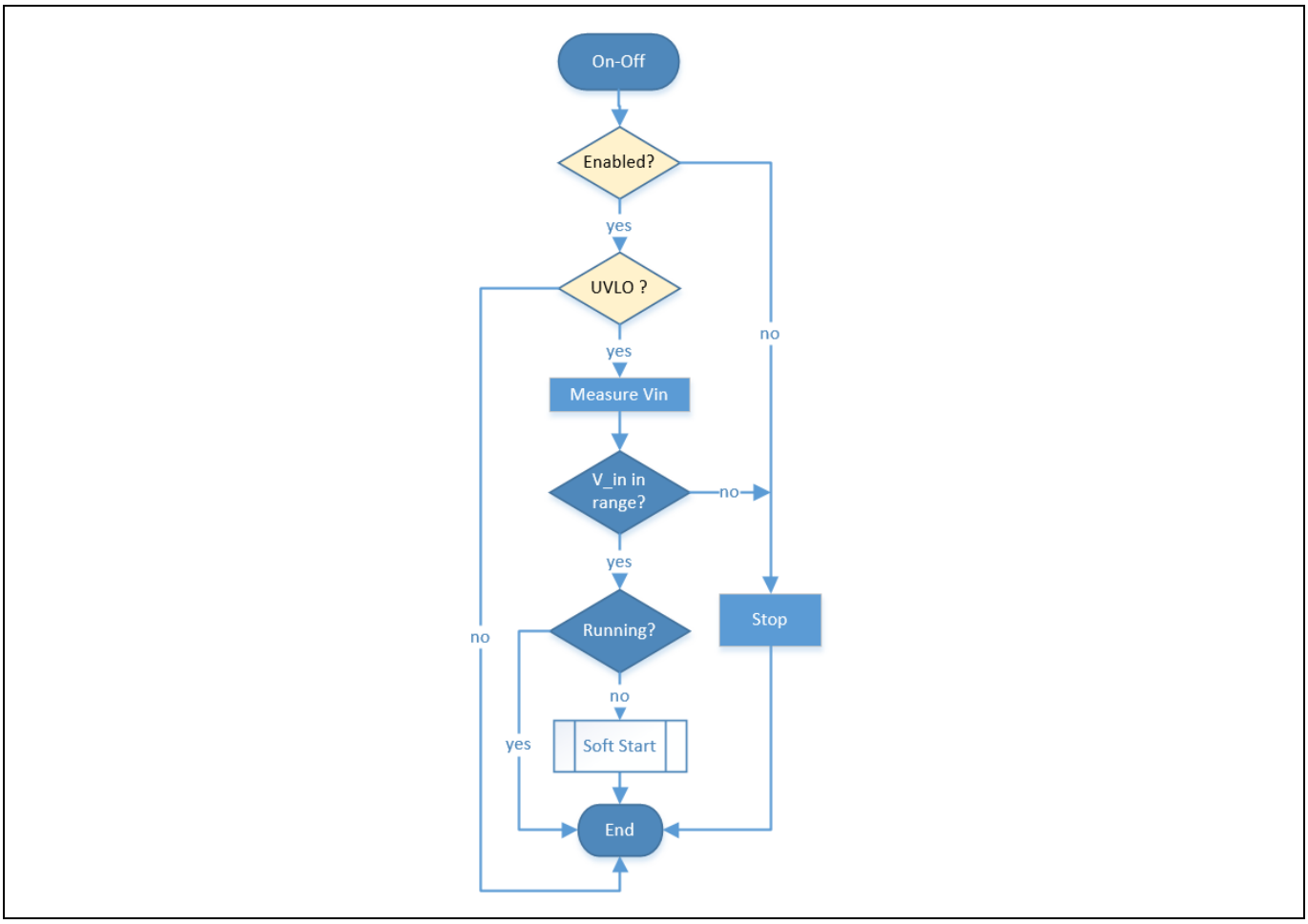


Figure 47 UVLO-OVLO and on-off flow diagram

4.6.4 Soft-start

The soft-start procedure ensures low stress on the devices when the output capacitor of the converter is discharged.

The soft-start sequence uses closed-loop regulation and ramps up the reference. The reference output voltage starts at the initial remaining value of the output capacitor and increases progressively in defined steps and defined delays (hard-coded into the firmware) up to the final nominal output (see Figure 49 and Figure 50).

The total duration of the soft-start sequence will depend on the compensation bandwidth, the size of the steps and the forced delays mentioned in the previous paragraph. For this application, as seen in Figure 48, soft-start at full load takes approximately 25 ms.

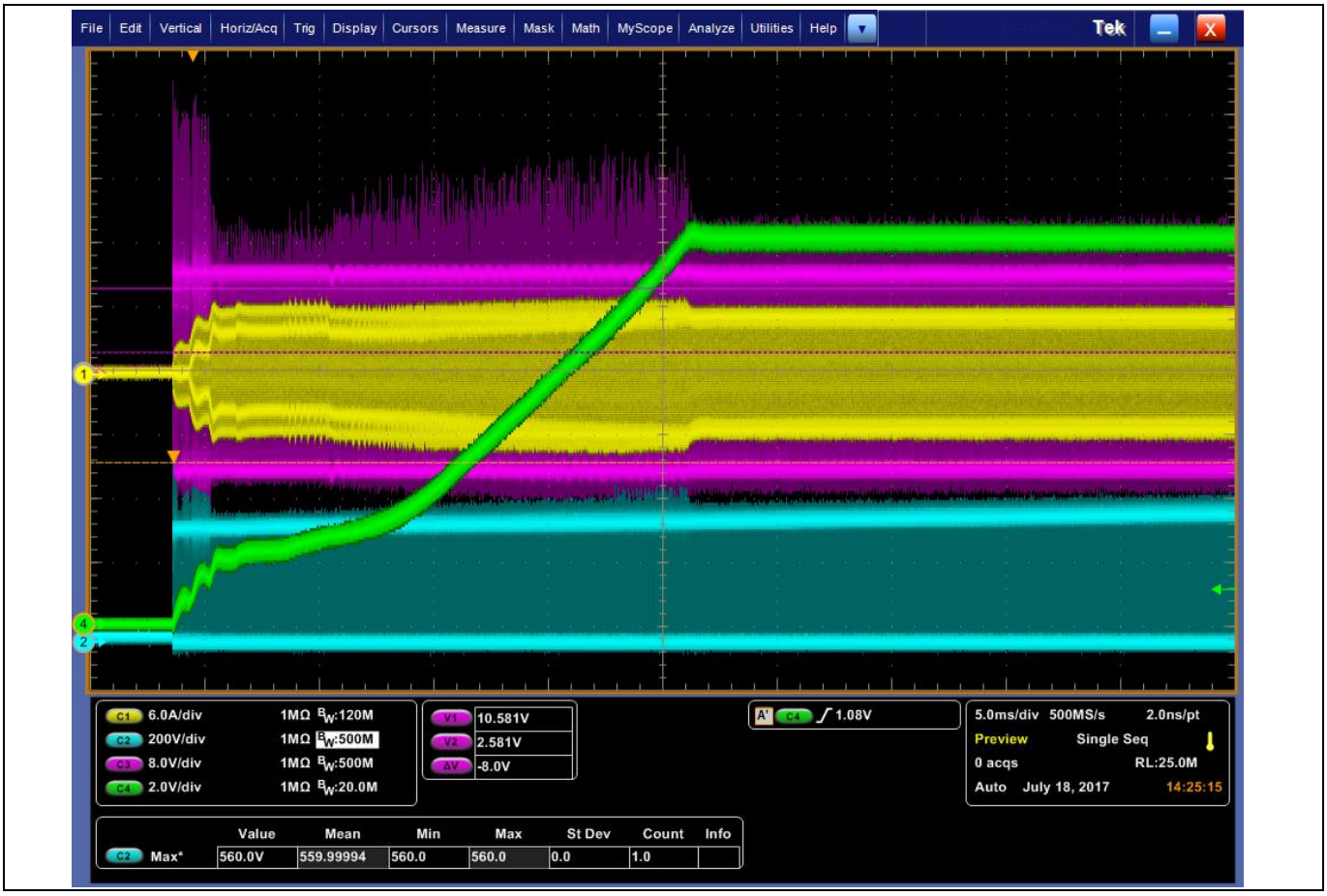


Figure 48 Soft-start at full load: primary current of transformer (yellow), output voltage of converter (green), V_{DS} of low-side full bridge MOSFET (blue) and V_{GS} of the same MOSFET (purple)

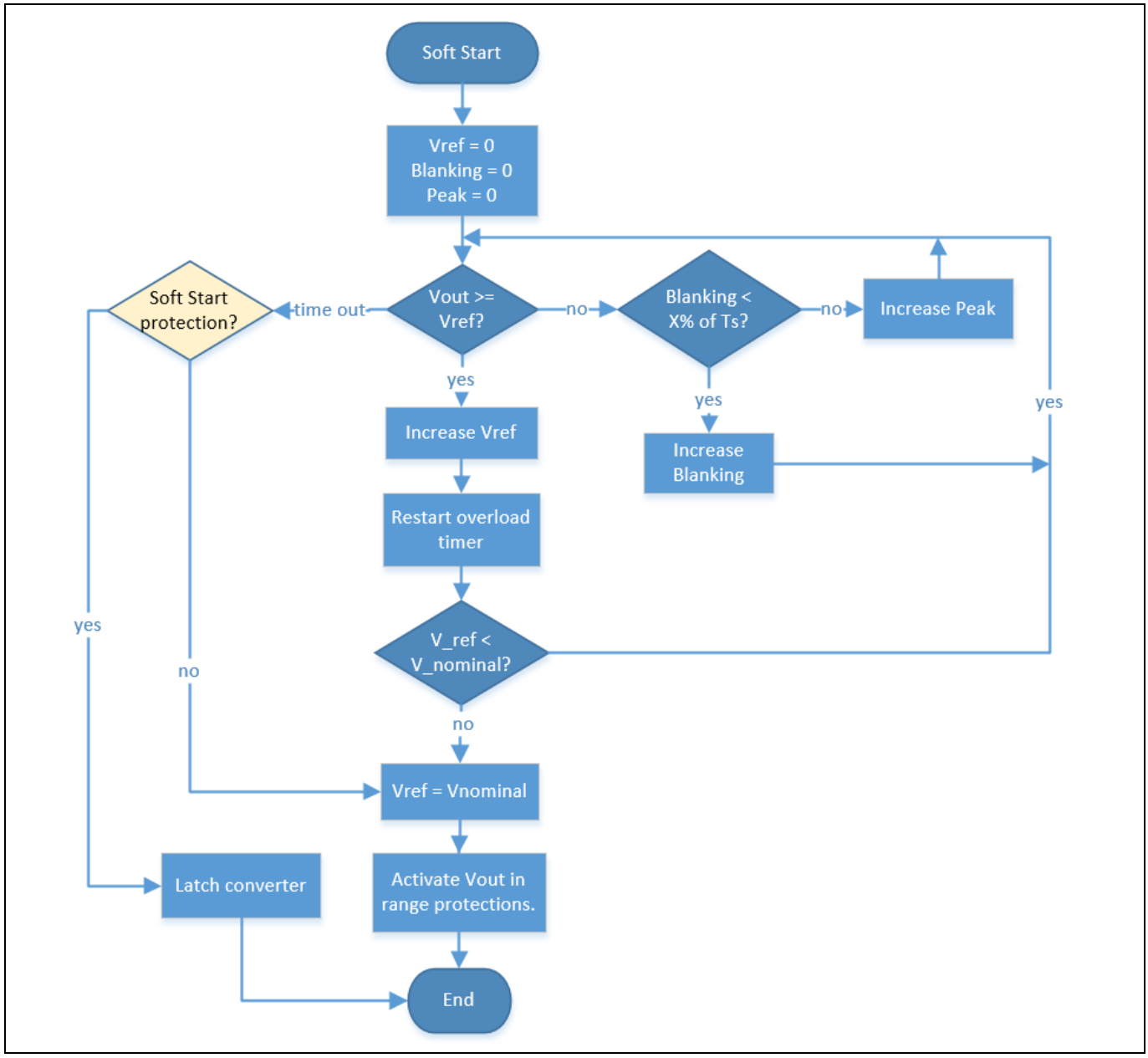


Figure 49 Soft-start procedure, PCMC

A timer would trigger an over-load protection if the output voltage does not rise. This protection will latch the converter.

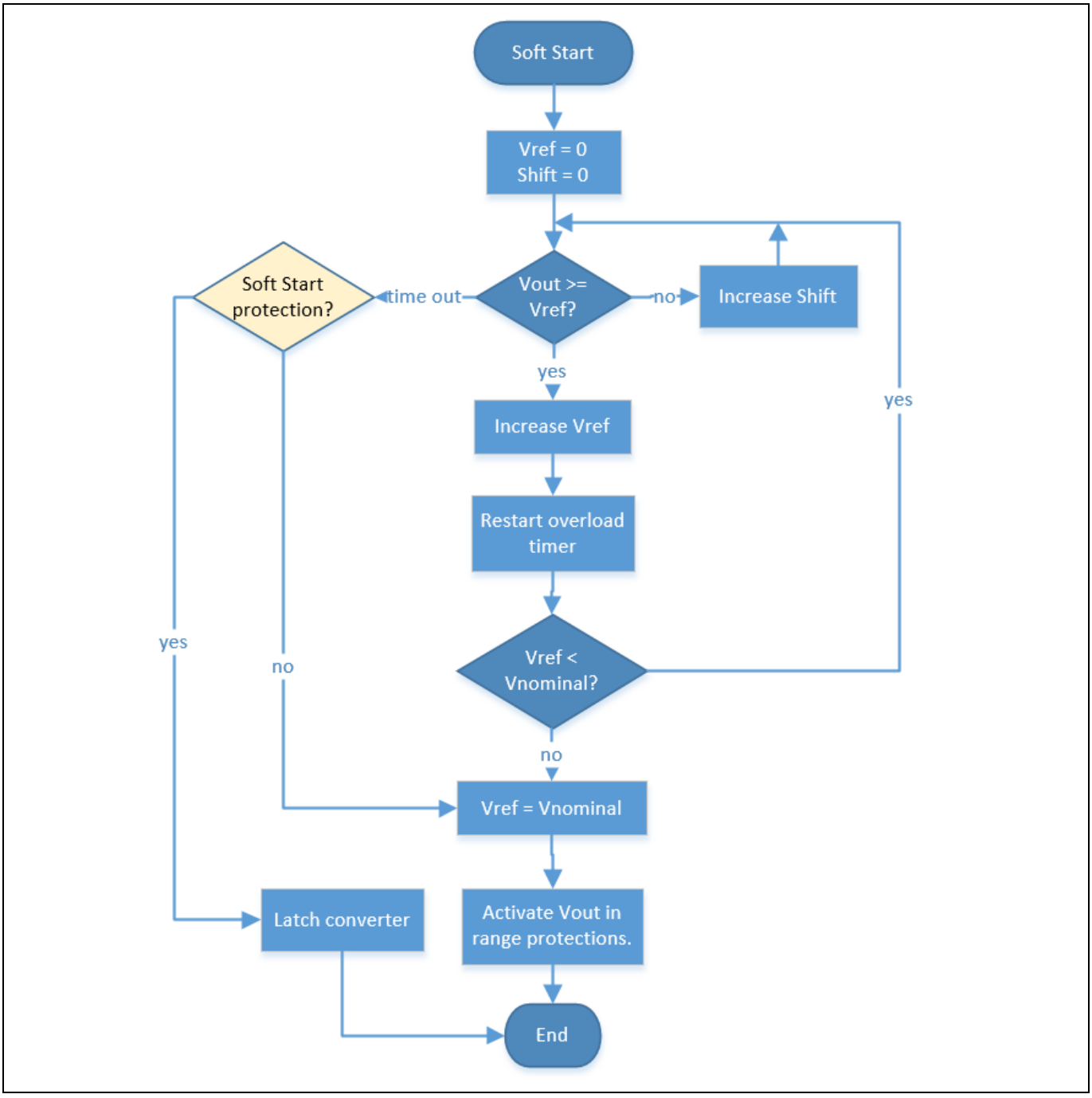


Figure 50 Soft-start procedure in VMC

In case of an OC event the converter will go into hiccup mode. Under extreme conditions, like short-circuit at start-up, a cycle-by-cycle peak current protection will prevent excessive stress on the system.

4.6.5 Output voltage out-of-range protection

Two main mechanisms protect the output voltage going out of the regulation window.

If the output voltage goes above 13.5 V the converter is latched. This will prevent excessive stress in the secondary LV devices and detect regulation problems (open-loop protection).

If the output voltage goes below 10.5 V the converter is latched (Figure 45). Output voltage will fall under this threshold under severe over-load conditions (short-circuit). This mechanism is an extra protection for the bridge and synchronous devices.

The output voltage nominal level can be cut from the GUI. However, the regulation window is hard-coded into the software (see Figure 51).

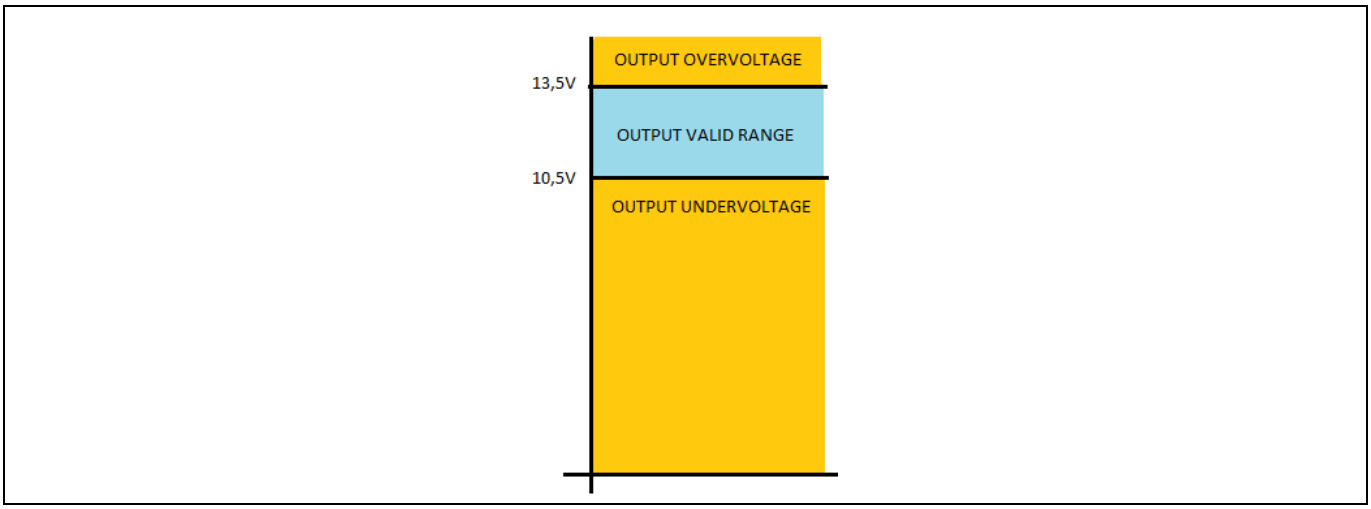


Figure 51 Output voltage out-of-range protection

4.6.6 Temperature control

A PWM-controlled variable-speed fan is mounted on-board, and air-flow will depend on the input current and/or temperature of the transformer (the hottest point of the design). The precedent is for the mechanism to require higher air-flow (see Figure 52).

The fan tachometer signal can be used to prevent a blocked rotor. If no tachometer is available, the protection can be deactivated in the GUI.

Note: Do not run the board without air-flow under heavy loads or during long intervals.

If the temperature of the transformer rises above the warning level the LEDs on the control card will blink with a specific pattern (see Figure 61). If the temperature increases above the warning range the converter will stop and latch. The warning and over-temperature levels are hard-coded into the firmware.

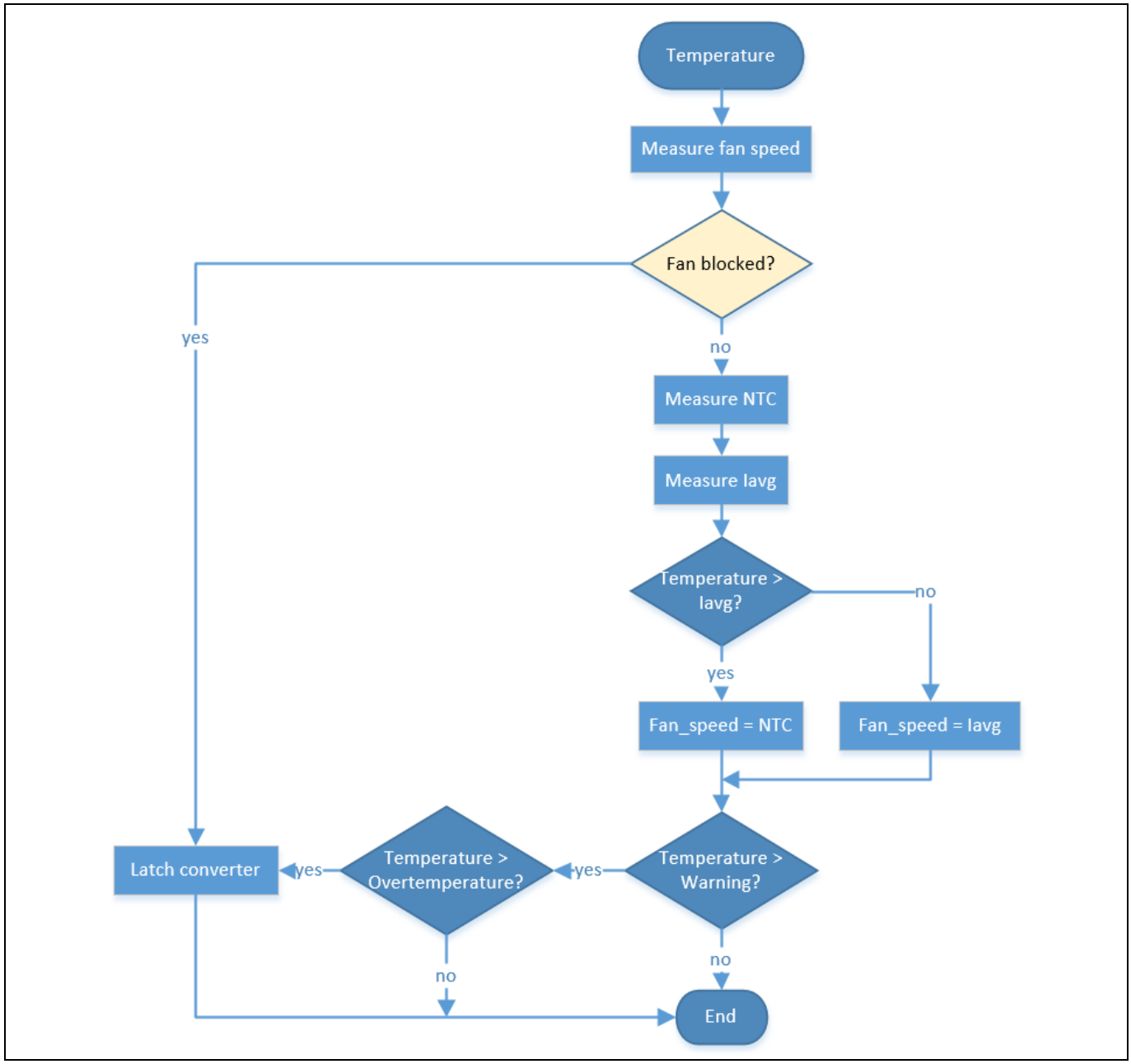


Figure 52 Temperature control flow diagram

4.7 User interface

The XMC42 controller includes communication peripherals with capabilities for UART, SPI and I²C protocols.

The PSFB 800 W control card uses serial communication (UART) to connect with an external system. We provide a GUI running in Windows as an example of remote management (see Figure 54). The serial interface provided with the kit can be used to link the converter to a Windows system via a USB port.

Note: *The GUI is optional, for possible customization or monitoring. The converter is fully operational when disconnected from the user interface.*

Note: *The controller implements a proprietary protocol with a reduced set of commands and message types not listed in this guide.*

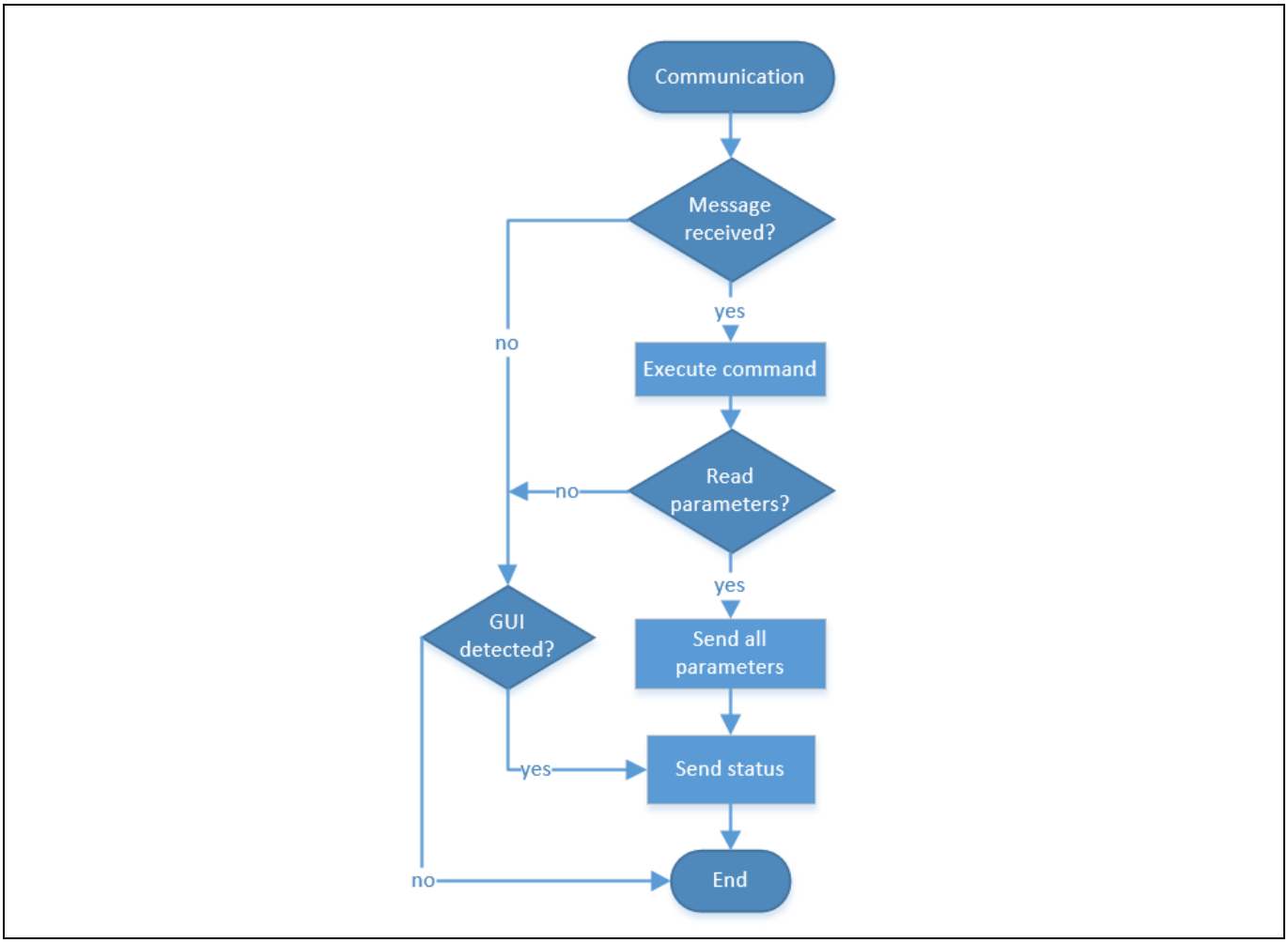


Figure 53 Communication routine flow diagram

Once the controller detects the connection with the GUI it will send the internal configuration of the converter, the current status and possible faults (see Figure 53).

Note: *This is an isolated HV system. Use an isolated serial communication port to connect the converter and a computer.*

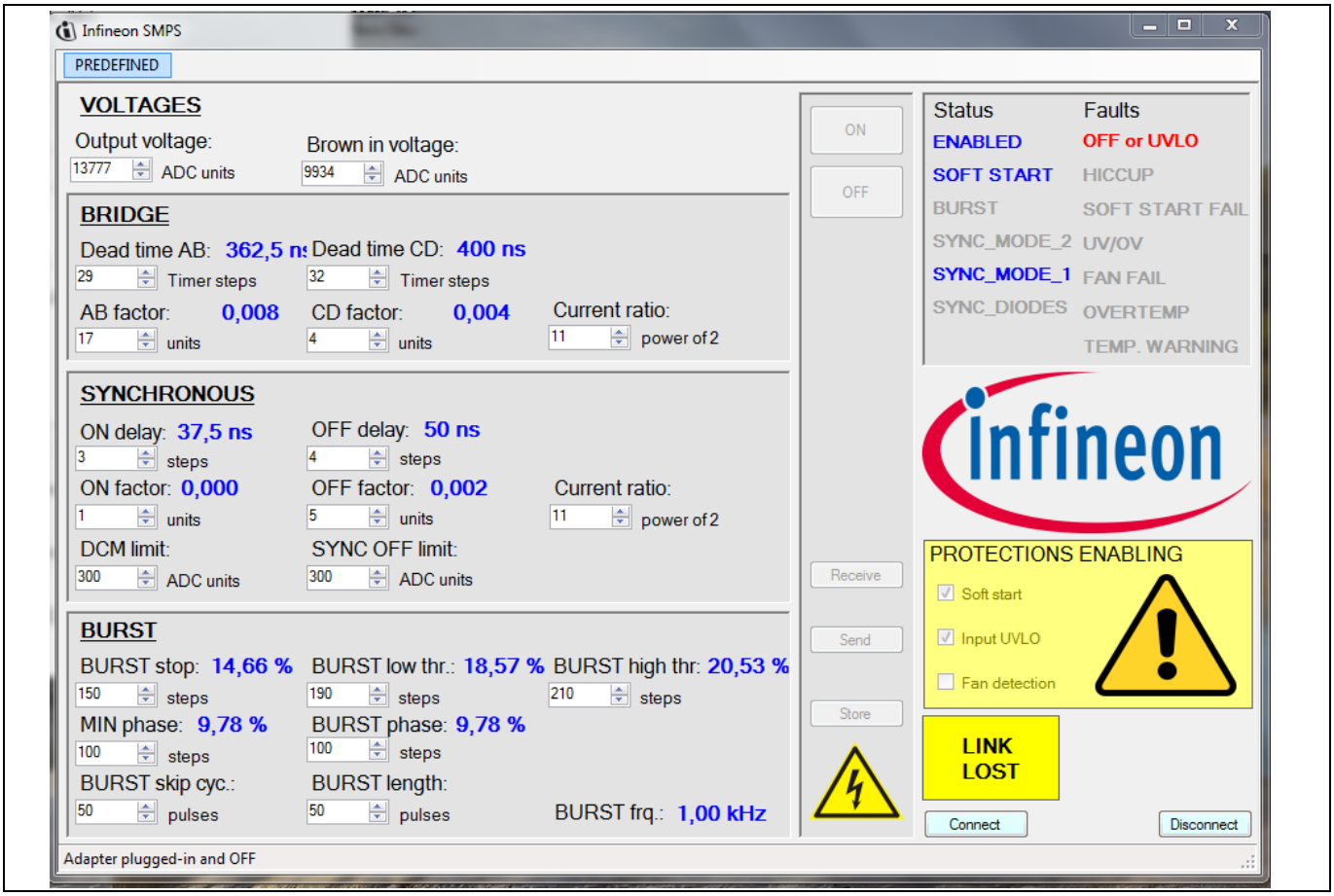


Figure 54 User interface detects the connection to a converter

The panels on the left contain configurable parameters for the converter firmware. The range for each of the values is limited both in the GUI and internally in the converter firmware, but a wrong combination of settings could lead to a system malfunction. The different settings are explained in more detail in the following sections.

The parameter values are permanently stored in the internal memory of the microcontroller. For storing the new values use the STORE button. Use the RECEIVE button for reading back the stored values and the SEND button for updating the microcontroller with the values in the GUI.

4.7.1 Status and faults

The status and faults panel is in the upper right-hand side of the GUI. Possible condition flags appear in faded gray. Flags will be highlighted if the condition applies.

Possible conditions are:

- ENABLED: If you use the OFF button a disable command is sent and the converter will stop (if running) and won't start even at the nominal input voltage range. Using the ON button means the ENABLED flag is highlighted again and the converter will run normally. The converter is enabled by default.
- SOFT-START: The converter runs the soft-start sequence.
- BURST: The converter is in burst mode.
- SYNC_M1: The synchronous rectifiers are in DCM mode (see 4.4.2).
- SYNC_M2: The synchronous rectifiers are activated and in normal mode 2 (see 4.4.3).

- SYNC_DIODES: The synchronous rectifiers are deactivated (see 4.4.1).
- OFF: The converter is off because a fault happened or because it was requested by the GUI. The converter will not run until the fault is removed or an ON command is requested.
- HICCUP: The converter is in HICCUP mode (see 4.6.1).
- SOFT-START FAIL: A soft-start failure happened (see 4.6.4).
- UV/OV: The output voltage has risen above or decreased below the valid range after reaching the regulation window (see 4.6.5).
- FAN FAIL: The signal from the fan tachometer is missing (see 4.6.6).
- OVERTEMP: Over-temperature detected. The converter is latched.
- TEMP. WARNING: The temperature of the converter is rising over the nominal conditions but the converter will keep running.

Note: The flags under STATUS are indicating different running modes. The flags under FAULTS indicate that the converter is switched OFF because of any of the faulty conditions.

4.7.2 Output voltage reference

This parameter adjusts the nominal output voltage of the converter (Figure 55). The parameter is in units of ADC sampled values in the range of 14 bits ([0, 16384]).

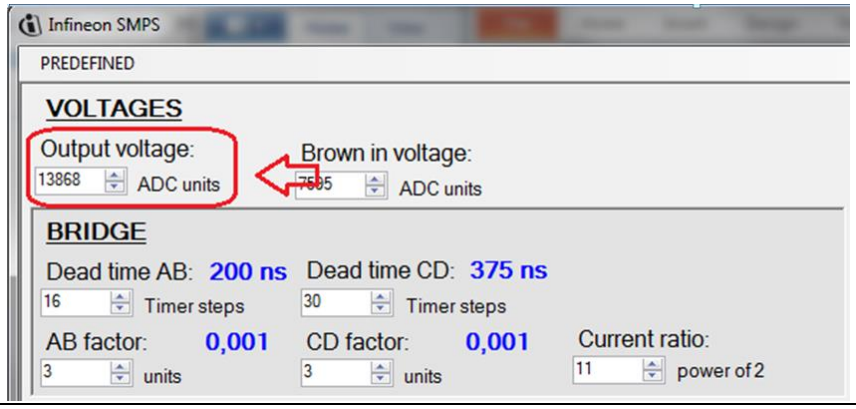


Figure 55 Output voltage nominal value

If the output voltage of the converter is not 12 V, adjust the parameter using the equation (25).

$$OUT_{newADC} = \frac{OUT_{presentADC}}{OUT_{newVoltage}} * OUT_{newVoltage} \quad (25)$$

4.7.3 UVLO-OVLO levels

This parameter sets the brown-in voltage of the converter. The parameter is in the units of ADC-sampled values in the range of 14 bits ([0, 16384]).

If the converter starts up at a different voltage than 350 V, adjust the parameter using the equation (26).

$$BROWN_IN_{newADC} = \frac{BROWN_IN_{presentADC}}{BROWN_IN_{currentVoltage}} * BROWN_IN_{newVoltage} \quad (26)$$

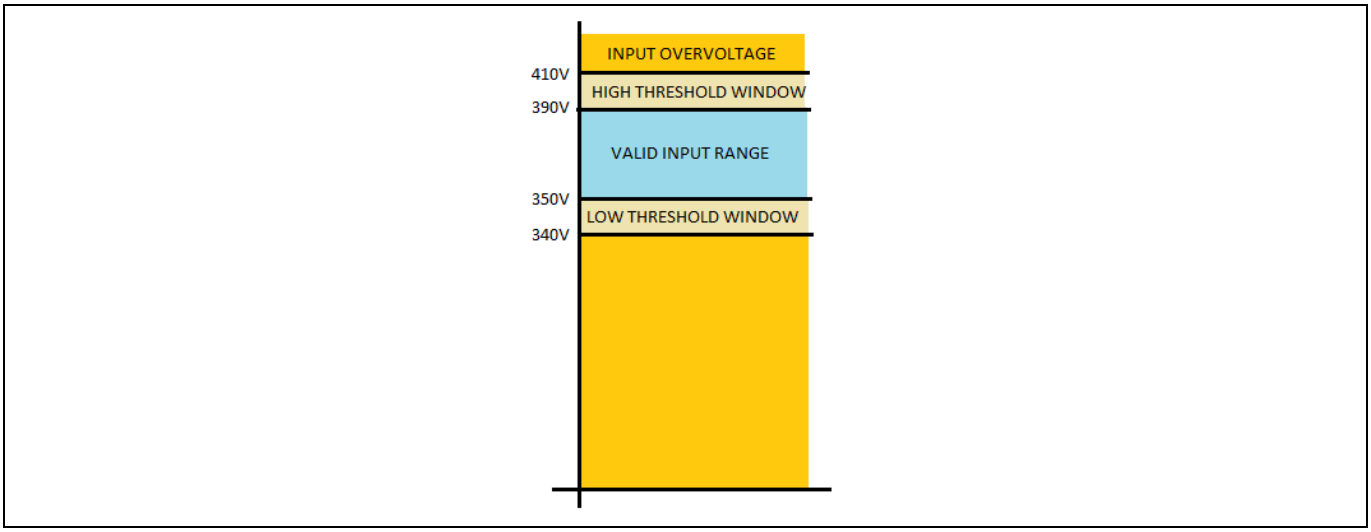


Figure 56 Input voltage range protection

The other input voltage thresholds are calculated by the controller based on the 350 V base level (Figure 56).

4.7.4 Bridge dead times

Dead-time settings for each of the legs in the bridge can be adjusted independently and on the fly.

The granularity of the values comes from the microcontroller timer clock period, in this case 12.5 ns. The minimum possible value is five steps, and the maximum is 255 steps.

Optimum dead times vary depending on load and input voltage. The relation can be approximated by a linear formula with the two parameters I_{factor} and I_{ratio}.

$$dt = dt_{nominal} - I_{in} * \frac{I_{factor}}{2^{I_{ratio}}} \quad (27)$$

The leading and lagging leg transitions behave differently. The leading leg has a resonant transition, with low variation of dead time along the load, and the lagging leg has a quasi-linear transition, much dependent on the load. Separate dead time, factor and ratio can be adjusted for each of the legs.

4.7.5 Synchronous rectifiers

On-delay (Figure 57) is the time added from the rising edge of A or B (start of the power transfer) and the rising edge of the gate of the corresponding synchronous branch.

Off-delay is the time added from the falling edge of C or D (end of the power transfer) and the falling edge of the gate of the corresponding synchronous branch.

Transition times vary with the load of the converter. The dependency can be approximated to a linear equation with two parameters: factor and ratio. The start and end of the power transfer behave differently; different factors and ratios apply for the turn-on and turn-off delay.

$$ON_{delay} = ON_{delay_nominal} - I_{in} * \frac{I_{factor}}{2^{I_{ratio}}} \quad (28)$$

$$OFF_{delay} = OFF_{delay_nominal} - I_{in} * \frac{I_{factor}}{2^{I_{ratio}}} \quad (29)$$

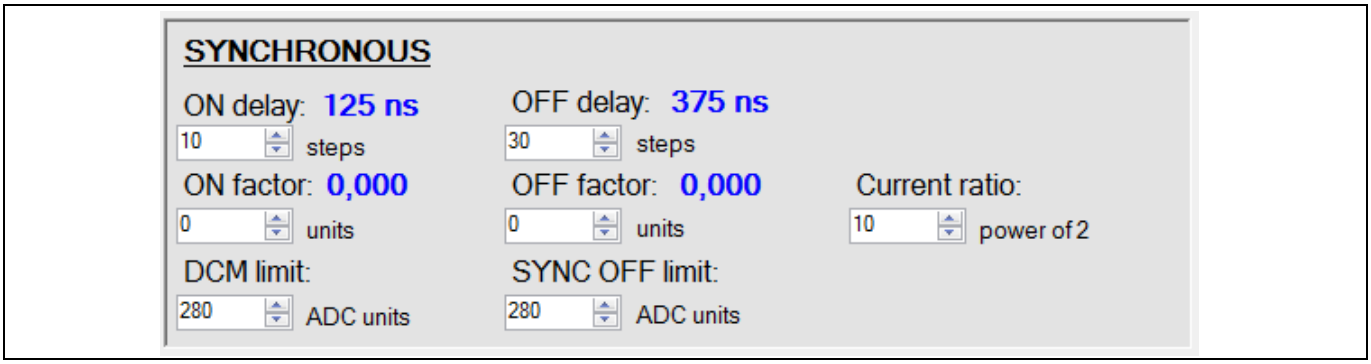


Figure 57 Delay of synchronous gate rising edge after drain voltage falling edge

There are several synchronous driving schemes (see 4.4) valid for different running conditions: DCM limit is the threshold for mode 2, the SYNC OFF limit is the threshold for mode 1, and below the SYNC OFF limit the synchronous MOSFETs are deactivated and behave as pure diodes (mode 0).

Note: The hysteresis window for the different modes is hard-coded into the firmware.

Values of the limit parameters SYNC OFF and DCM account for average input current, in the range of 14 bits ([0, 16384]).

4.7.6 Burst mode thresholds

The burst driving scheme further improves efficiency under light-load or no-load conditions at the expense of increased output ripple (see 4.5).

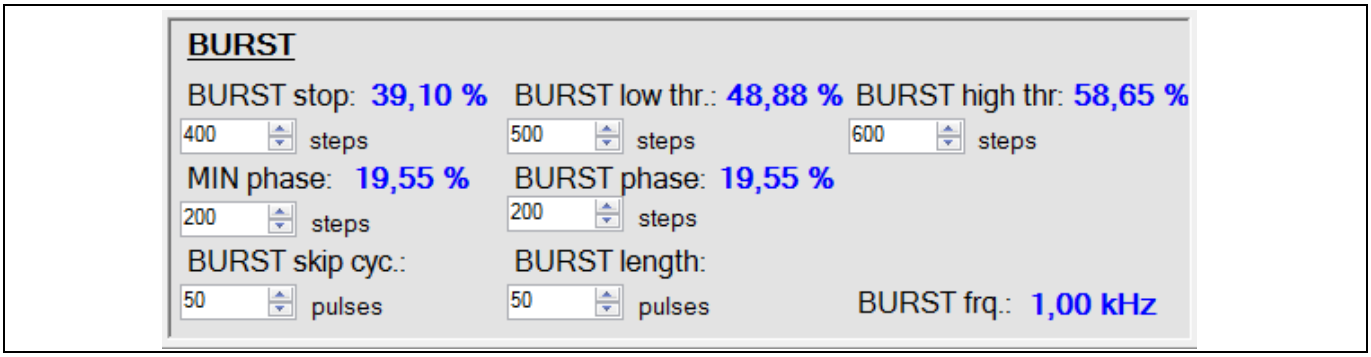


Figure 58 Burst mode thresholds

The different parameters, described in 4.5, determine how the burst scheme behaves: output ripple, burst frequencies, audible noise.

4.7.7 Protections

Some protections can be deactivated for debugging purposes or special testing cases. The protections deactivating panel is on the right-hand side of the GUI (see Figure 59).

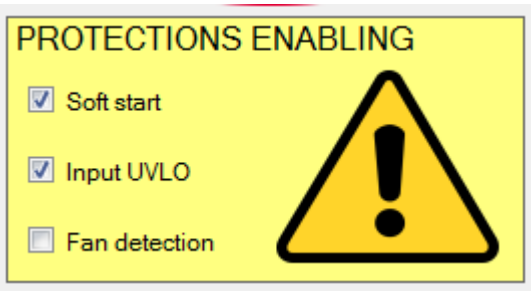


Figure 59 Soft-start protection enabling

Note: Clicking in the check boxes sends the new configuration to the microcontroller, but for the change to be effective after a power recycle use the STORE button.

The soft-start check box deactivates the soft-start sequence time-out protections.The converter can be operated out of nominal conditions, starting from low input voltages and increasing progressively.

The UVLO check box deactivates the input voltage out-of-range protections. The converter will operate at any input conditions.

The fan detection check box deactivates the fan tachometer detection. Fan modulation control is still active, but there is no detection of a broken rotor (temperature protection is always active).

4.7.8 Storage of parameters in Flash

XMC42 on-chip Flash memory can be used as permanent storage. Firmware itself has writing and reading access to the Flash memory, which makes the use of an external Electrically Erasable Programmable Read-Only Memory (EEPROM) unnecessary.

Areas of the memory can be reserved for this special purpose. Firmware can be updated and the reserved sections will remain unmodified.

The parameters can be written or read through the communication interface (UART in this case), under the control of the firmware in the microcontroller, or through the programming interface in a mass-production use case.

4.7.9 LEDs on the daughter card

Three LEDs are mounted on the control card to provide status information from the converter and control card.

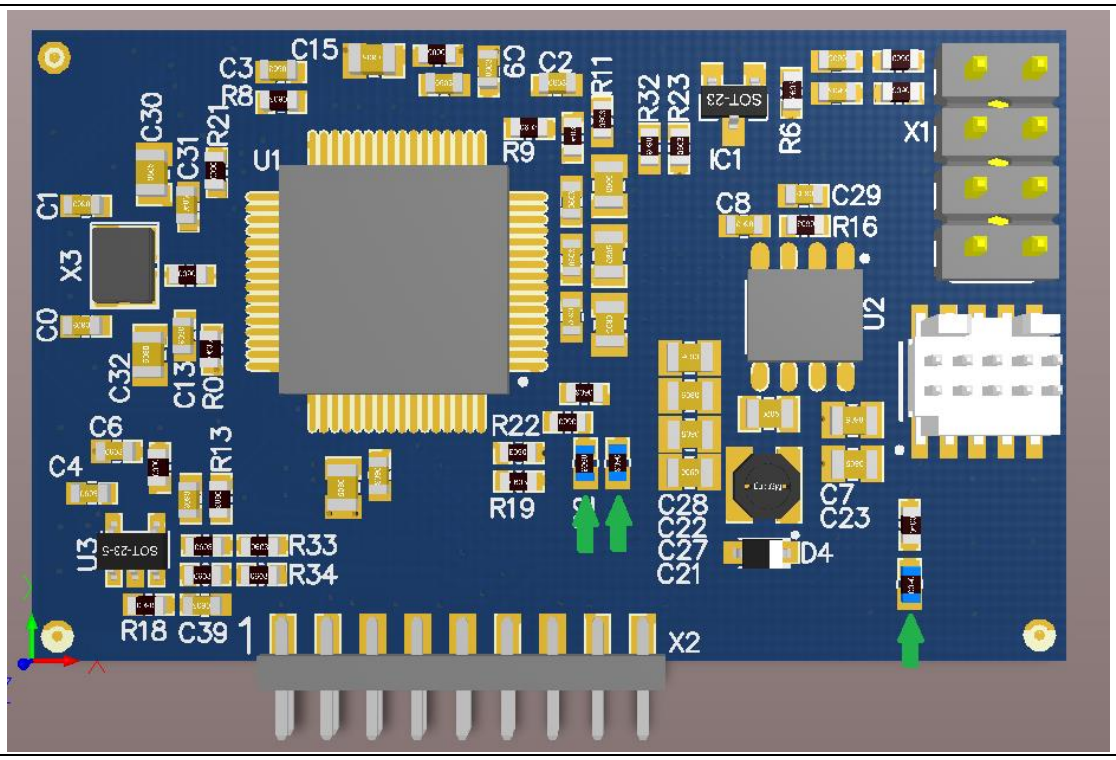


Figure 60 Control card on-board LEDs (green arrows)

The LED in the bottom right-hand corner shows power present in the controller circuitry (3.3 V).

The two other LEDs are used to indicate the status or fault information of the converter. Messages are coded by the color of the LEDs and by a blinking pattern.

- Temperature fault: measured temperature of the converter above the limit. The protection latches the converter. Power has to be recycled to remove latching protections.
- Soft-start time-out: over-load during soft-start sequence.
- No fan pulses detected: the signal from the tachometer of the fan is missing. If a fan without sensor is used, or the fan is powered externally, deactivate the fan protection.
- Output OV/UV: output voltage out of the regulation window after reaching regulation (see 4.6.5).
- Temperature warning: measured temperature of the converter is high. This is not a fault, but status information.
- Running with no faults: if the converter is running (input voltage in range) and none of the other conditions apply.
- Brown-out: none of the other conditions apply, and the input voltage is out of range.

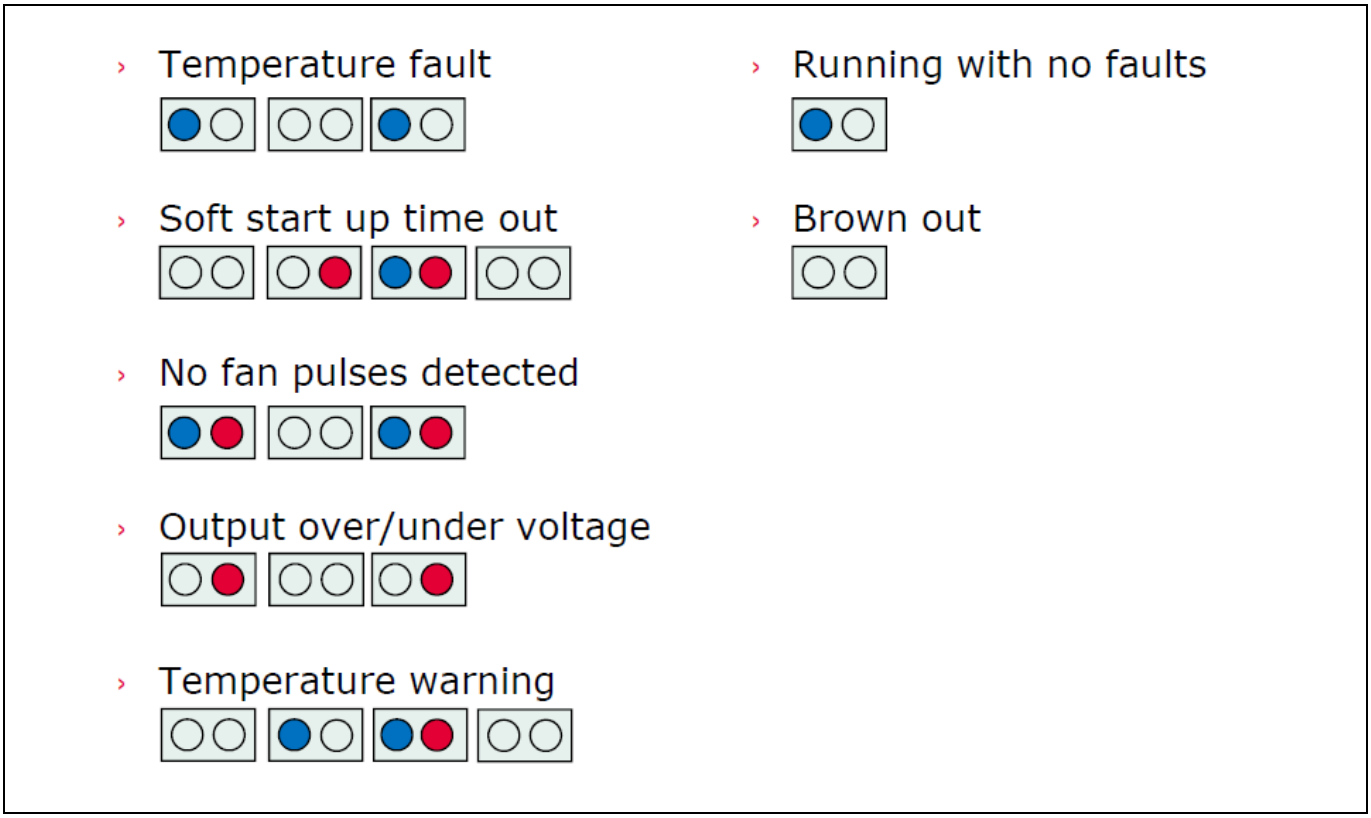


Figure 61 **A square frame represents one of the states of the sequence. A blue dot means a blue LED is lit. A red dot means a red LED is lit. Sequence states are changing at 2 Hz.**

5 Performance evaluation

5.1 Primary MOSFETs ZVS

The waveforms are captured with reference to the nomenclature used in section 2.1.1 “Principle of operation.”

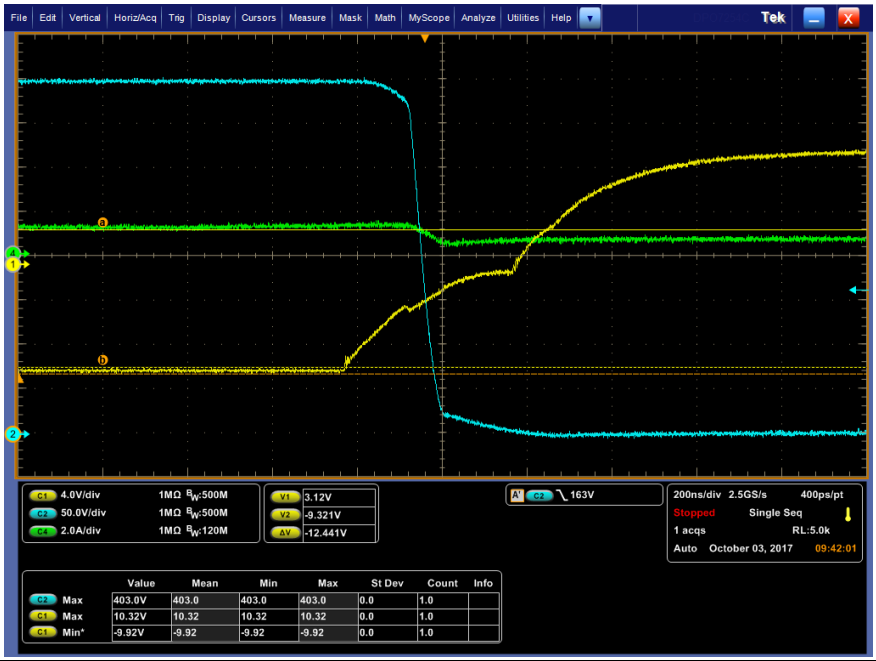


Figure 62 Lagging leg achieves ZVS at I_{out} = 24 A. Waveforms captured on MOSFET D: V_{DS} (blue); V_{GS} (yellow); primary current (green).

Figure 62 shows the turn-on of the low-side MOSFET in the lagging leg (D) at the minimum load current needed to achieve the ZVS. This corresponds to around 20 percent of full load, as in the original design target. The ZVS behavior is as usual clearly recognized by the absence of Miller Plateau in the V_{GS} waveform.

The following Figure 63 shows the turn-on of the low-side MOSFET in the leading leg (B), which is able to achieve the the ZVS at full load. This target is the best trade-off between the efficiency target at light load (in our case dictated by the 80Plus® Platinum® standard) and the amount of resonant inductance needed, which may have some impacts on the mid- and full-load efficiency, due to copper losses in the windings. In any case the resonant tank design and the related dead-time settings are optimized for the IPP60R170CFD7 device.



Figure 63 Leading leg achieves ZVS at 117 A. Waveforms captured on MOSFET B: V_{DS} (blue); V_{GS} (yellow); primary current (green).

5.2 SR MOSFETs operation

5.2.1 Synchronous MOSFETs dead time

In the second driving scheme (see 4.4.3) BD conduction is kept down to a minimum, but still maintaining a safety margin, so as not to overlap drain voltage, and an active channel.

During turn-off transition of the synchronous rectifier, the rise of the voltage in the drain is delayed as a function of the load and the input voltage of the converter (the time it takes for the primary-side current to reverse direction). The controller implements a linear approximation of the relation, which can be parametrized to keep the turn-off margin constant at different loads (Figure 64, Figure 65 and Figure 66).

One can appreciate that at any load condition the peak voltage is well below 80 percent of the MOSFET voltage rating (80*0.8 = 64 V), according to the typical derating guidelines applied in the SMPS design: this contributes to optimizing the so-called Mean Time Between Failures (MTBF), an important index of SMPS reliability.



Figure 64 Synchronous turn-on/off delay at 140 W load. V_{DS} (purple) and V_{GS} (blue).

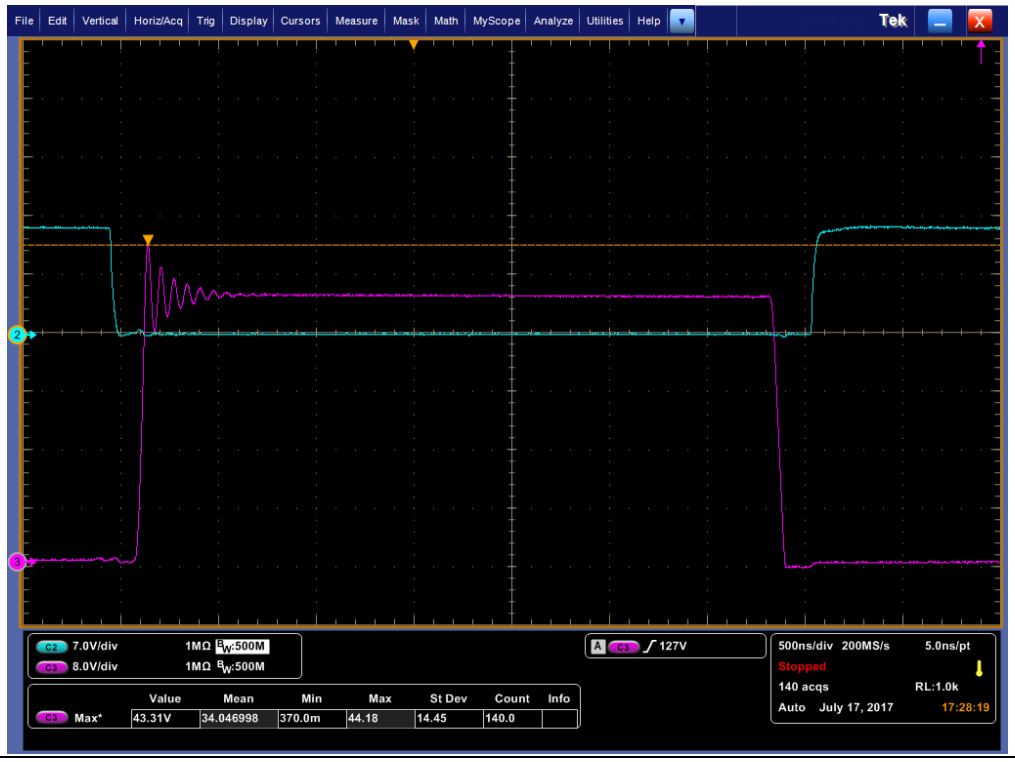


Figure 65 Synchronous turn-on/off delay at 700 W load. VDS (purple) and V_{GS} (blue).

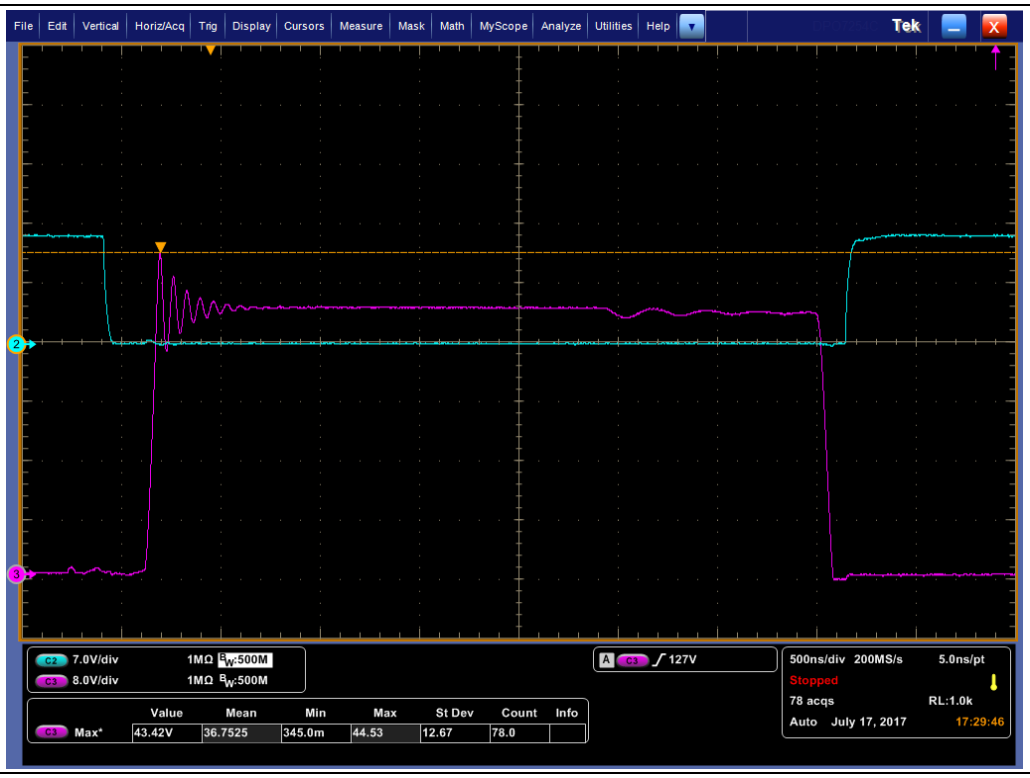


Figure 66 Synchronous turn-on/off delay at 1400 W load. V_{DS} (purple) and V_{GS} (blue).

The turn-on transition delay is also influenced by the load and input voltage of the converter, but because of the time for the lagging leg bridge transition. During the turn-on dead time, most of the current is conducted by the other branch, so timing is not as critical as for the turn-off transition (Figure 67).

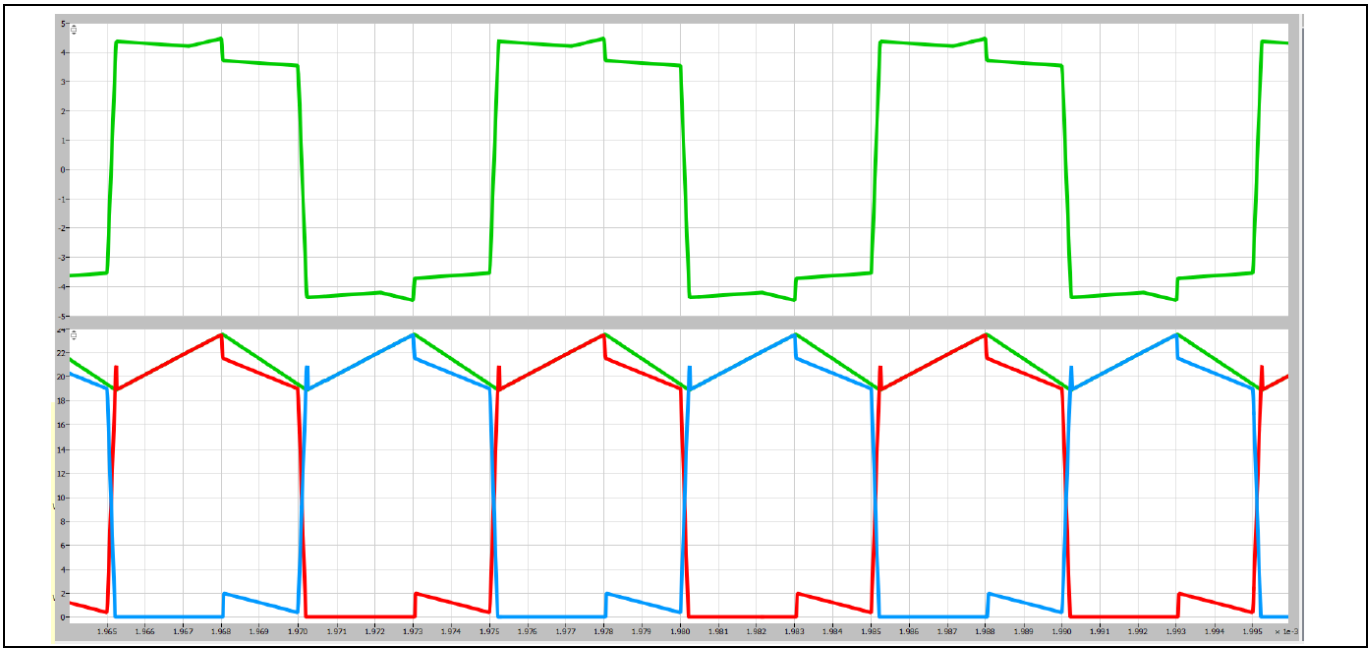


Figure 67 Current through SR branches. Primary current of transformer (top green), output choke current (bottom green), SR branches current (red and blue).

5.3 Short-circuit protection

A very important protection in a ZVS PSFB converter is the one against output short-circuit. This is because historically there have been many problems associated with this condition, as already mentioned in the introductory paragraph 2.1.

For that reason we consider the waveforms captured during this condition particularly relevant.

Figures 68–70 show the most severe short-circuit conditions in a ZVS PSFB, even including start-up under short-circuit. Both primary current and MOSFET_V_{DS} are reported to show especially that the second one remains well below the MOSFET ratings during these abnormal conditions. This minimizes the risk of excessive stress on the device, thus ensuring a very reliable converter operation.



Figure 68 **Start-up under short-circuit conditions. Primary current (yellow), V_{DS} of low-side MOSFET (purple) and output voltage of converter (blue).**

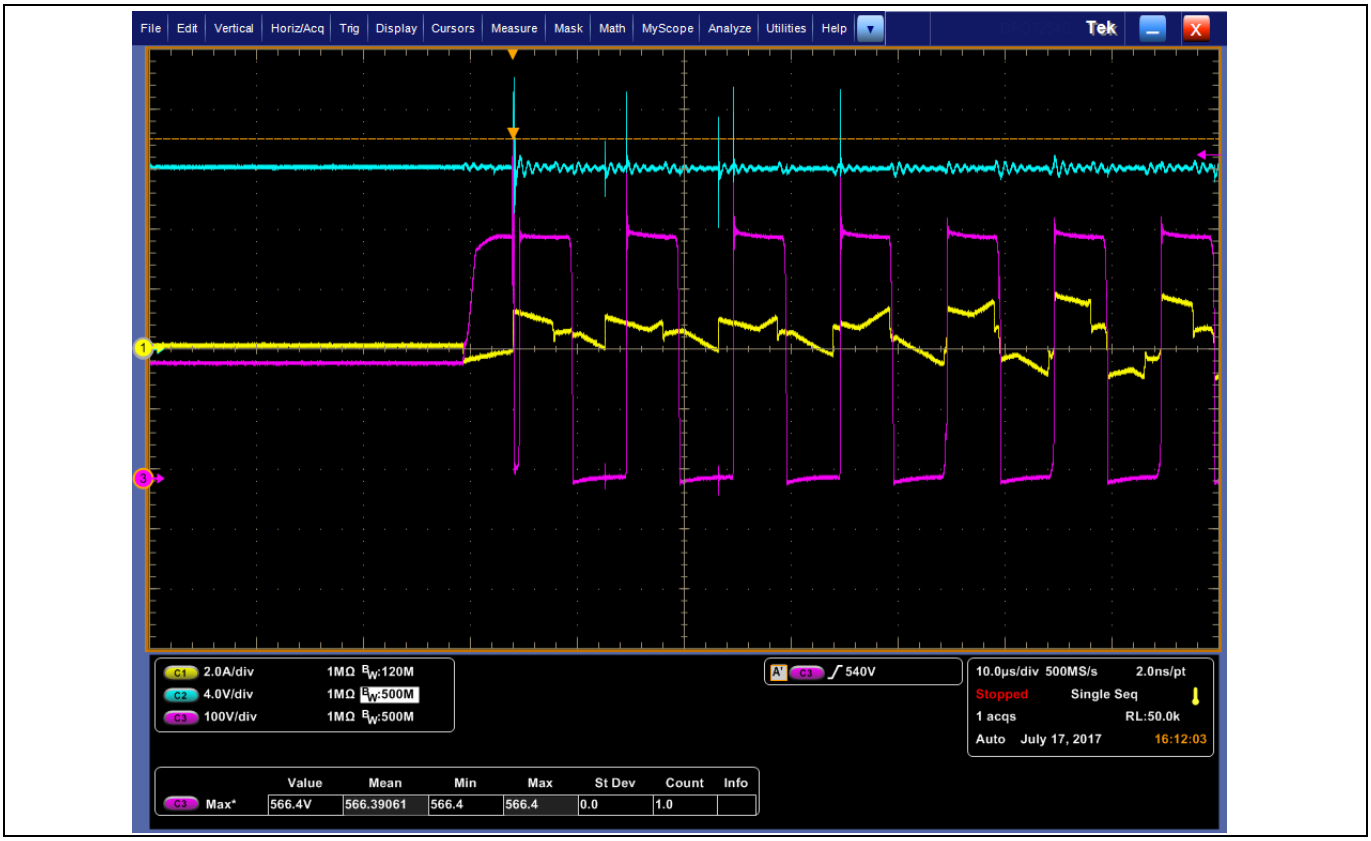


Figure 69 **Short-circuit under no load at output. Primary current (yellow), output voltage (blue), MOSFET V_{DS} (purple).**



Figure 70 **Short-circuit under full-load conditions at output. Primary current (yellow), MOSFET V_{DS} (purple), output voltage (blue).**

5.4 Dynamic loading

Figure 71 and Figure 72 report the typical dynamic load waveforms according to the converter's spec.

The outcome of those waveforms is that the output over-shoot and under-shoot are always below the specified 400 mV_{pk-pk}.

In the plots below the output voltage during a dynamic load is shown in AC coupling, in order to highlight the related over-shoot and under-shoot. The plotted current (in yellow) is the primary one corresponding to the secondary current change.

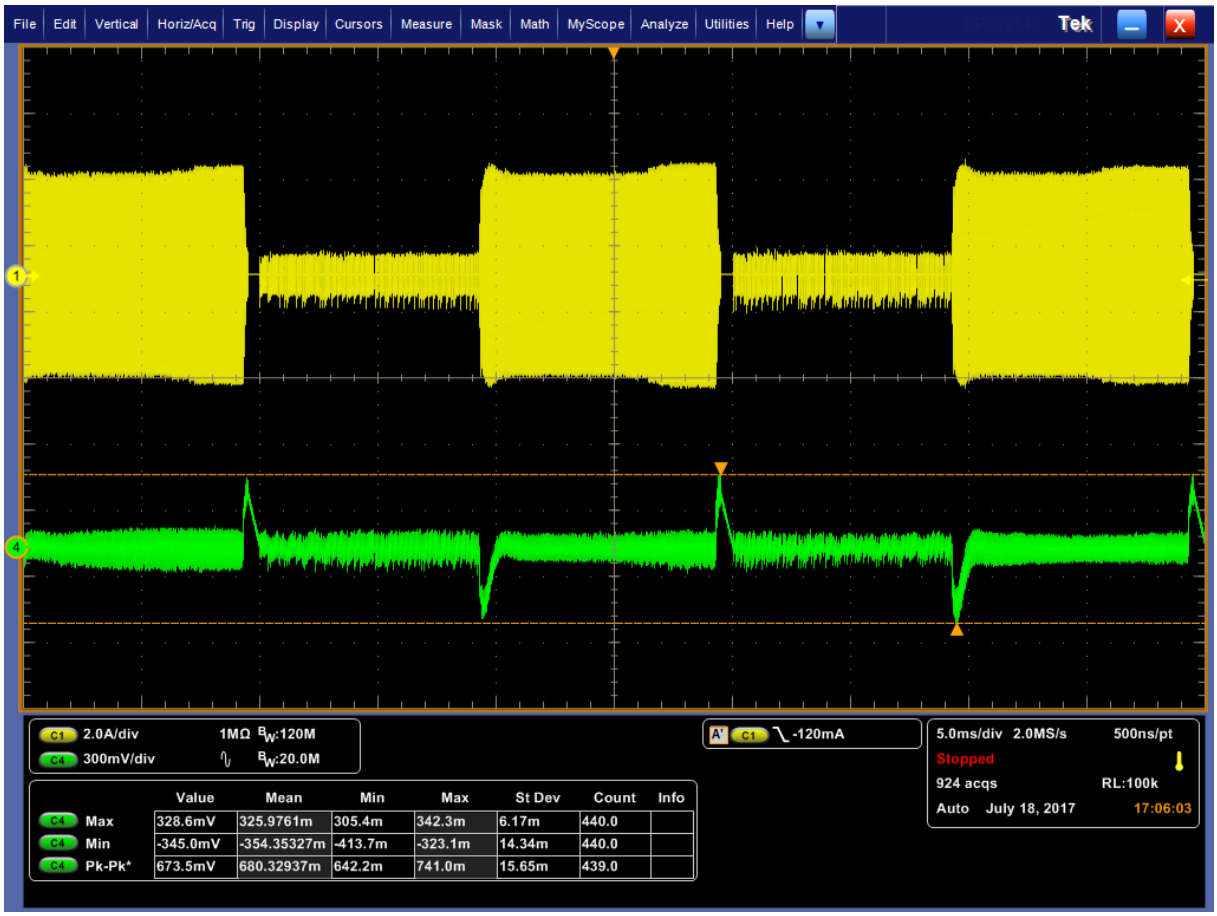


Figure 71 5 A–60 A output dynamic load. Primary current (yellow), output voltage (green).



Figure 72 60 A–117 A output dynamic load. Primary current (yellow), output voltage (green).

5.5 Efficiency plot: CFD7 design optimization

This section provides some guidelines on ways to optimize the performance of the CFD7 technology in the ZVS PSFB topology. It is shown that following these guidelines will enable the best efficiency plot and the best switching behavior of the device, which also means the most reliable operation.

Three design parameters are particularly important on this purpose:

- The total gate resistance seen by the device in the turn-on and turn-off paths ($R_{G,on}$ and $R_{G,off}$)
- The primary dead-time setting
- The SR secondary delay time setting

In order to limit channel conduction during turn-off, and thus reducing the associated losses, it is best to use a very low $R_{G,off}$ resistance: in fact, $R_{G,off}$ = 0 Ω has ben used by default in our design, in order to make the turn-off as fast as possible, which results in the best efficiency.

The selection of $R_{G,on}$ is more critical, since it involves several aspects.

Generally, higher $R_{G,on}$ values help to reduce the di/dt generated at MOSFET turn-on, which translates to reduced dv/dt = L_{stray} × di/dt experienced by the turn-off device. This is very important especially at light-load operation, when ZVS may be lost during turn-on.

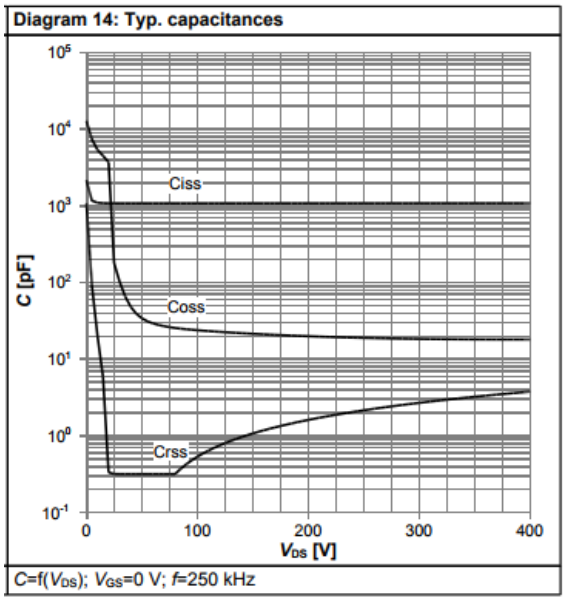


Figure 73 Typical MOSFET capacitances

On the other hand, the HB turn–off device operates in the high C_{GD}/C_{GS} region of its characteristics (see Fig. 73 as a reference), so it is more exposed to the dv/dt feedback effect on the gate through the C_{GD}. Thus heavy oscillations can be potentially generated both on the V_{DS} and V_{GS} of the turn-off device, with the possibility of re-turn-on and the consequent increase in switching losses. Figures 74 and 75 show the effect of two different values of $R_{G,on}$ (15 Ω and 75 Ω) on CFD7 switching behavior during start-up at no load and I_{out} = 10 A conditions. You can see the smoother waveforms measured with $R_{G,on}$ = 75 Ω, which means a greater margin with reference to the MOSFET ratings, but also higher efficiency at least at light-load operation.

IPP60R170CFD7

- $R_{g,on}$ = 15 Ω
- $V_{ds(max)}$ = 484.0 V
- $V_{gs(min)}$ = -14 V
- $V_{gs(max)}$ = 29.28 V
- $V_{gs_plateau_ringing\ (max)}$ = 10.88 V



IPP60R170CFD7

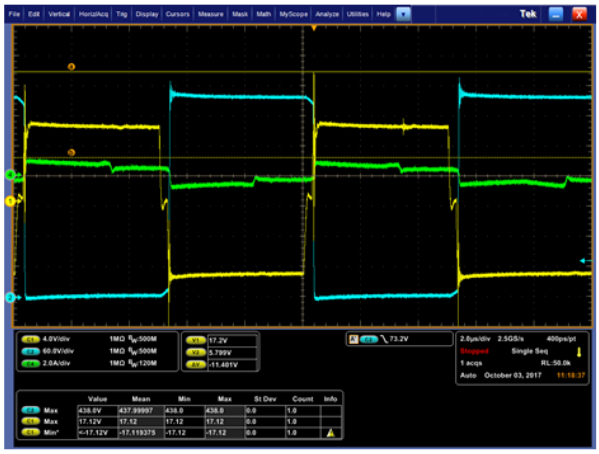
- $R_{g,on}$ = 75 Ω
- $V_{ds(max)}$ = 428.8 V
- $V_{gs(min)}$ = -14 V
- $V_{gs(max)}$ = 18.4 V
- $V_{gs_plateau_ringing\ (max)}$ = 7.4 V



Figure 74 **Effect of different values of $R_{G,on}$ on CFD7 switching behavior during start-up at no load. V_{DS} (blue); V_{GS} (yellow); primary current (green).**

IPP60R170CFD7

- $R_{g,on}$ = 15 Ω
- $V_{ds(max)}$ = 438 V
- $V_{gs(min)}$ = -17.12V
- $V_{gs(max)}$ = 17.12 V
- $V_{gs_plateau_ringing\ (max)}$ = 17.12 V



IPP60R170CFD7

- $R_{g,on}$ = 75 Ω
- $V_{ds(max)}$ = 416.0 V
- $V_{gs(min)}$ = -11.8 V
- $V_{gs(max)}$ = 11.6 V
- $V_{gs_plateau_ringing\ (max)}$ = 7.4 V

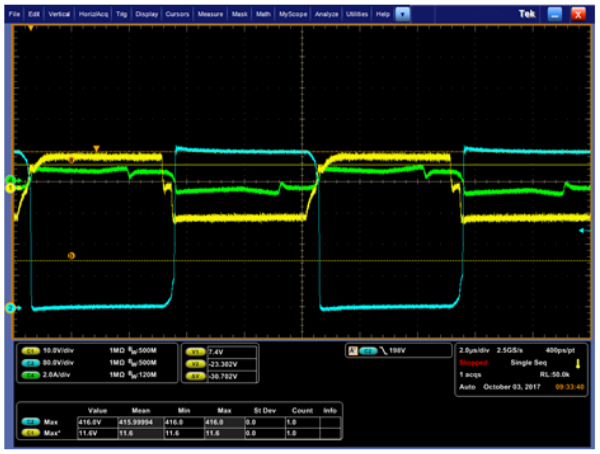


Figure 75 **Effect of different values of $R_{G,on}$ on CFD7 switching behavior at I_{out} = 10 A. V_{DS} (blue): V_{GS} (yellow); primary current (green).**

This is confirmed by the comparative efficiency plots measured using $R_{G,on}$ = 15 Ω and $R_{G,on}$ = 75 Ω respectively for each of the four devices in the full bridge (see Figures 76 and 77).

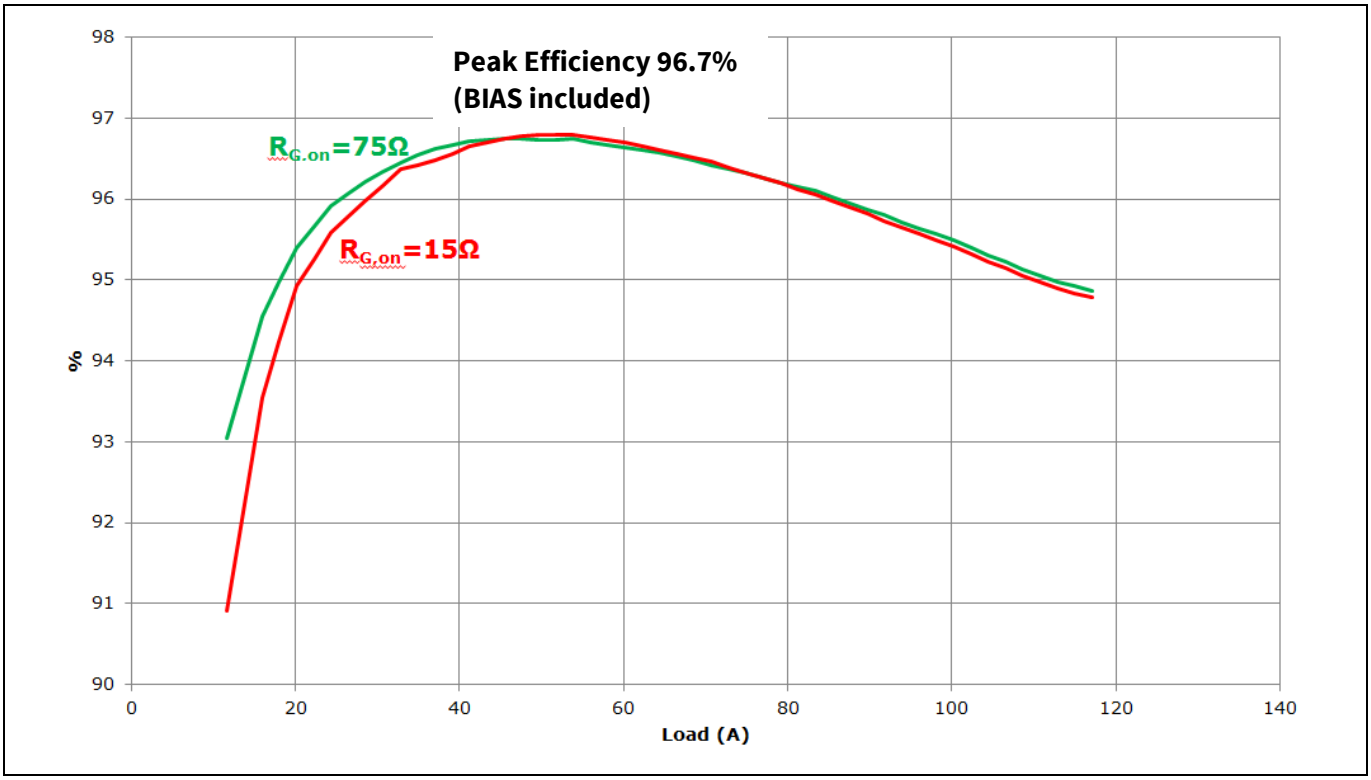


Figure 76 Effect of different values of $R_{G,on}$ on IPP60R170CFD7 efficiency plot in 1400 W demo board

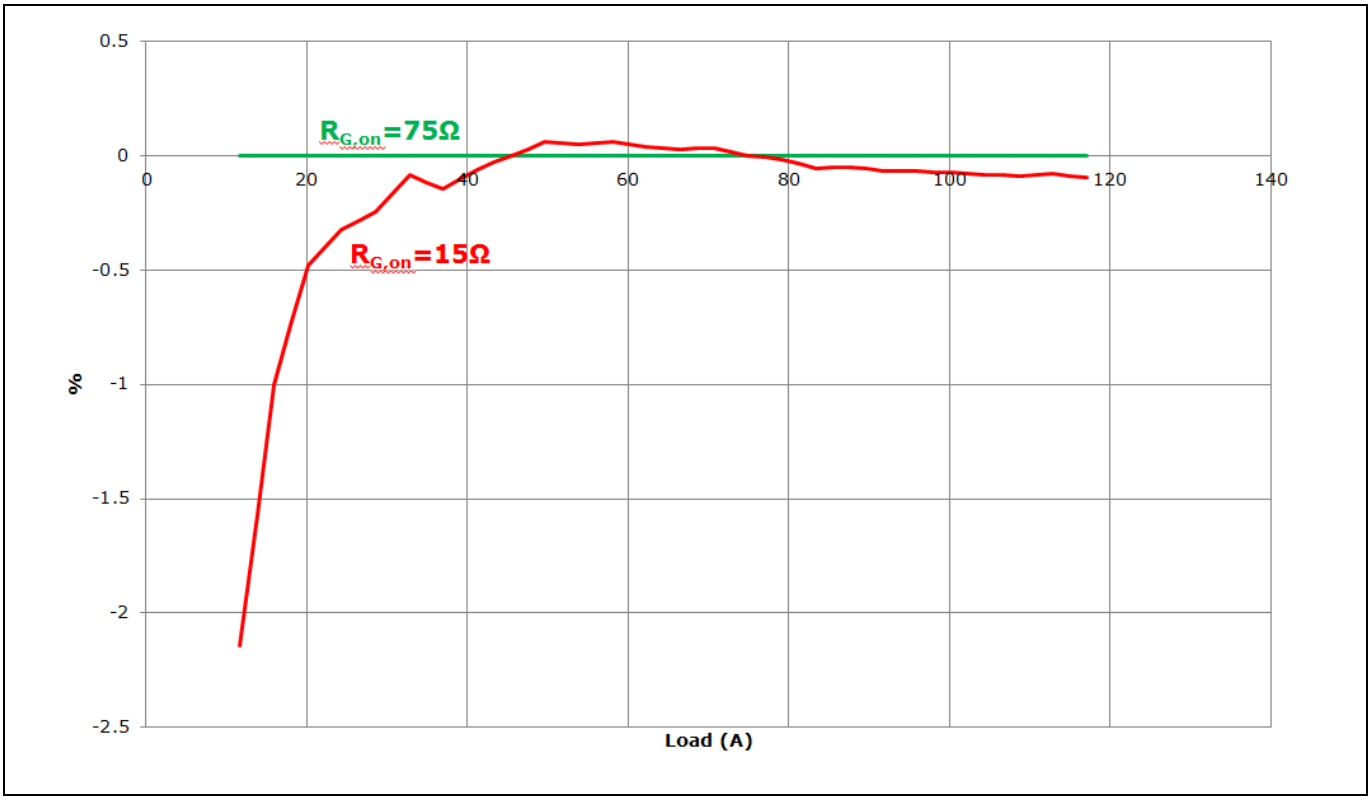


Figure 77 Effect of different values of $R_{G,on}$ on IPP60R170CFD7 efficiency plot in 1400 W demo board (Δη)

The efficiency plots reported in Figures 76 and 77 have been measured with a fully automated set-up and following the typical procedures prescribed by the 80Plus® Platinum® standard (see [12] for more details).

The better switching behavior enables significantly higher efficiency below 30 percent load when $R_{G,on}$ = 75 Ω is used, without any significant impact on the higher loads. At 10 percent load the difference is really striking: more than 2 percent higher efficiency when $R_{G,on}$ = 75 Ω is selected compared to $R_{G,on}$ = 15 Ω.

It is important to mention that the dead time on the primary side and the SR delay times have been re-adjusted with the help of the GUI according to the different values of $R_{G,on}$. This is done in order not to compromise any ZVS behavior and keep optimal SR operation; otherwise we would generate different loss mechanisms, which would certainly affect the overall efficiency.

Figure 78 shows the efficiency comparison between IPP60R170CFD7 and two major competitor parts in a comparable $R_{DS(on)}$ range. The measurements have been done in the CFD7-optimized design, as described above in this paragraph.

A very impressive result is that IPP60R170CFD7 is more efficient compared to Competitor A and Competitor B over the entire load range, with an outstanding improvement between 1.4 percent and 1.8 percent at 10 percent load.

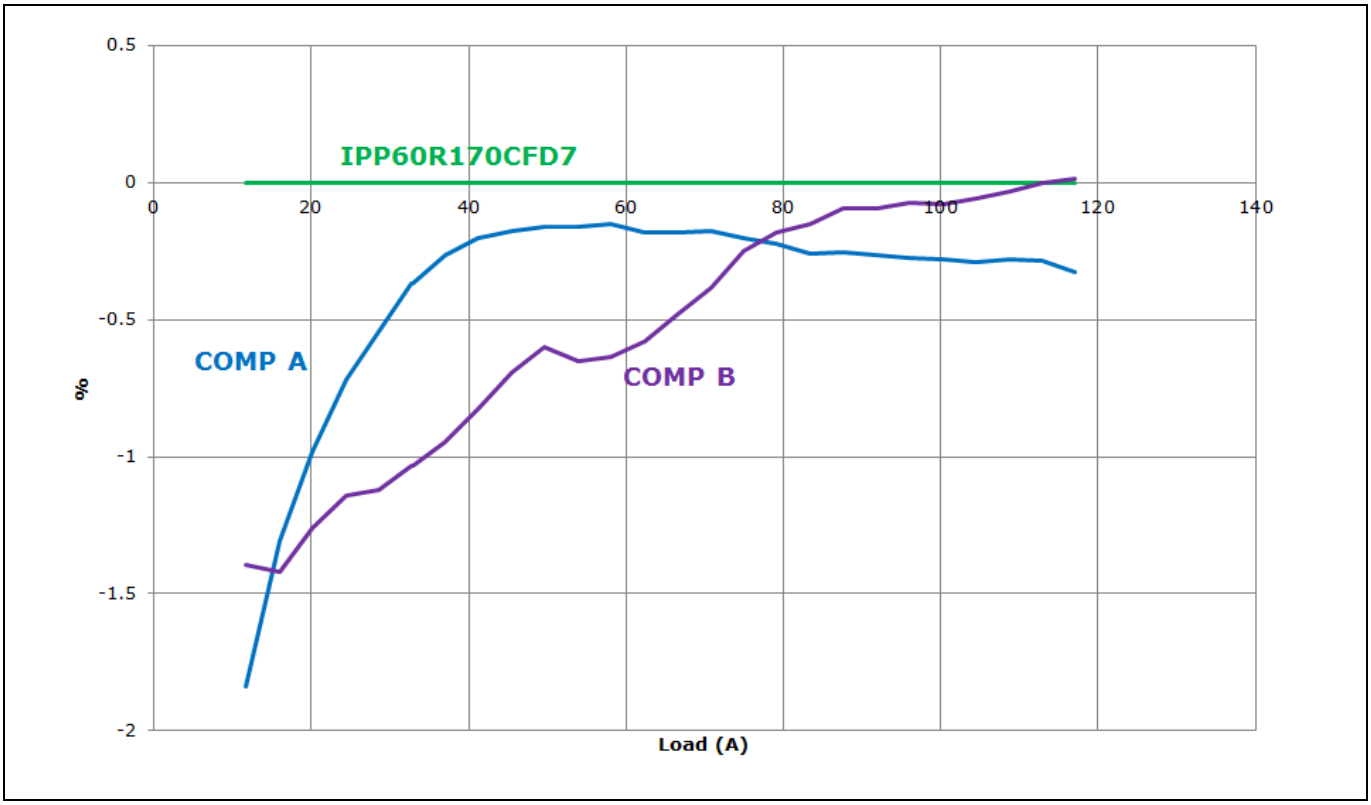


Figure 78 Efficiency comparisons of the 1400 W ZVS PSFB evaluation board: CFD7-optimized design

Figure 79 compares the best efficiency achieved by CFD7 in a CFD7-optimized design and by the Competitor A device in a Competitor A-optimized design. Even in this comparison CFD7 shows significantly higher efficiency across the whole load range, especially at 10 percent load (+1.4 percent).

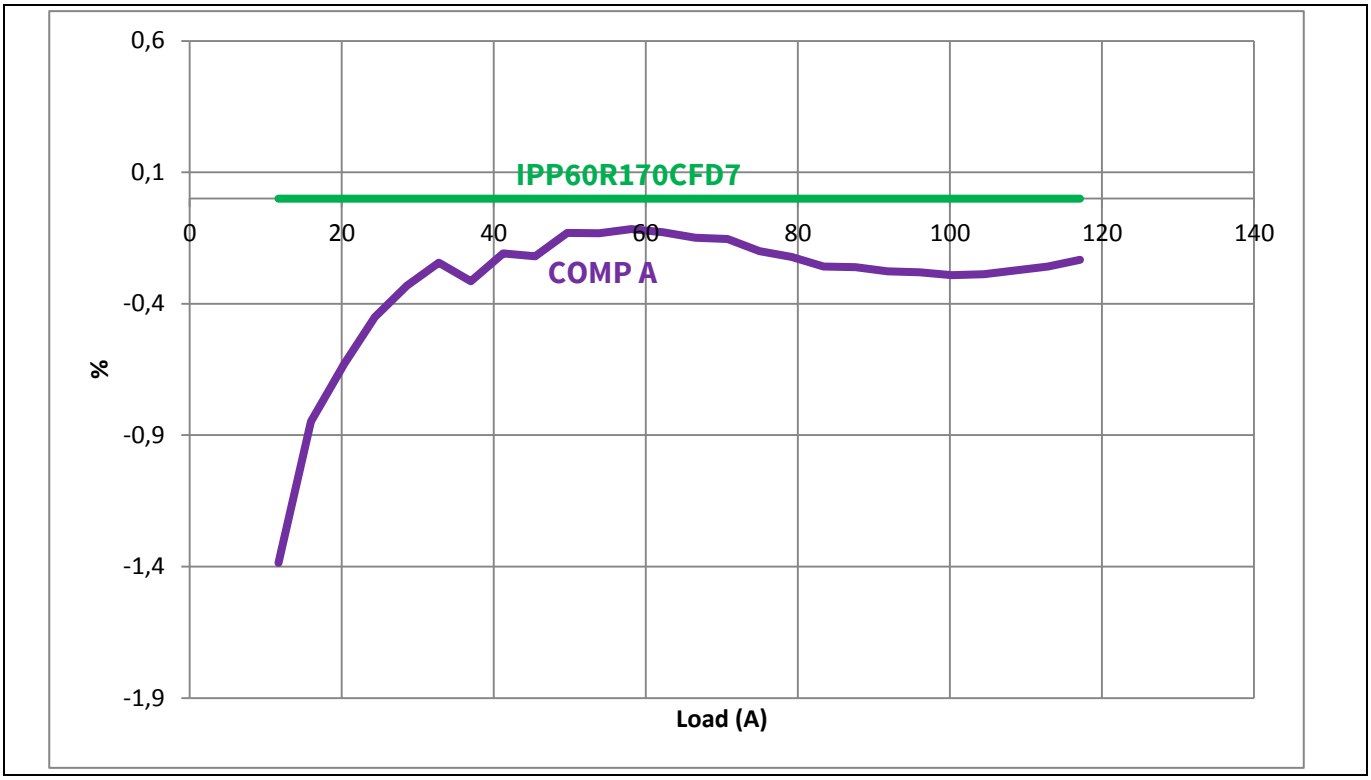


Figure 79 Efficiency comparisons of the 1400 W ZVS PSFB evaluation board: CFD7-optimized design vs Competitor A-optimized design

The key takeaways of this analysis can be summarized as follows:

- Every time a new MOSFET technology is tested in the ZVS PSFB topology, optimization of the driving circuit, including the re-adaptation of delay times, is needed in order to get the best device performance.
- Replacing a MOSFET in a design already optimized for another MOSFET in the same $R_{DS(on)}$ range in a simple “plug and play” approach may not enable the best performance of the new device.
- A good trade-off can be normally achieved in the design in order to get satisfactory behavior from both devices and a good balance between performance and reliability.

In any case, the achieved peak efficiency at 50 percent load (around 96.7 percent including the bias absorption) is the best possible, with +12 V output with the ZVS PSFB topology. This value is in fact comparable with the peak efficiency achievable with fully resonant topologies like HB or FB LLB at +12 V output. Moreover, the fixed-frequency and duty-cycle operation of the ZVS PSFB are features which make intrinsically easier the HV DC/DC power conversion control, expecially in industrial battery charger applications, in comparison with a fully resonant approach.

Overall the efficiency plot shows a certain flatness, and in the end it is compatible with the requirements of the 80Plus® Platinum® standard in combination with a suitable PFC-stage efficiency.

5.6 Thermal maps



Figure 80 Board thermal map at 100 percent load (117 A) at room temperature (~24°C)

Figure 80 shows that the primary full bridge heatsink stabilizes at around 24°C. This very low temperature is the result of the new CFD7 technology, its efficient driving concept and the cooling applied.

The hotspot on the board is the transformer with around 65°C. Main losses within the transformer are coming from the secondary copper, whose temperature exceedes 96°C at 24°C ambient tempeerature, as can be seen in the detailed map in Figure 81. This value is acceptable, since the proper operation of the transformer, including the primary-to-secondary safety isolation, is guaranteed up to 130°C.

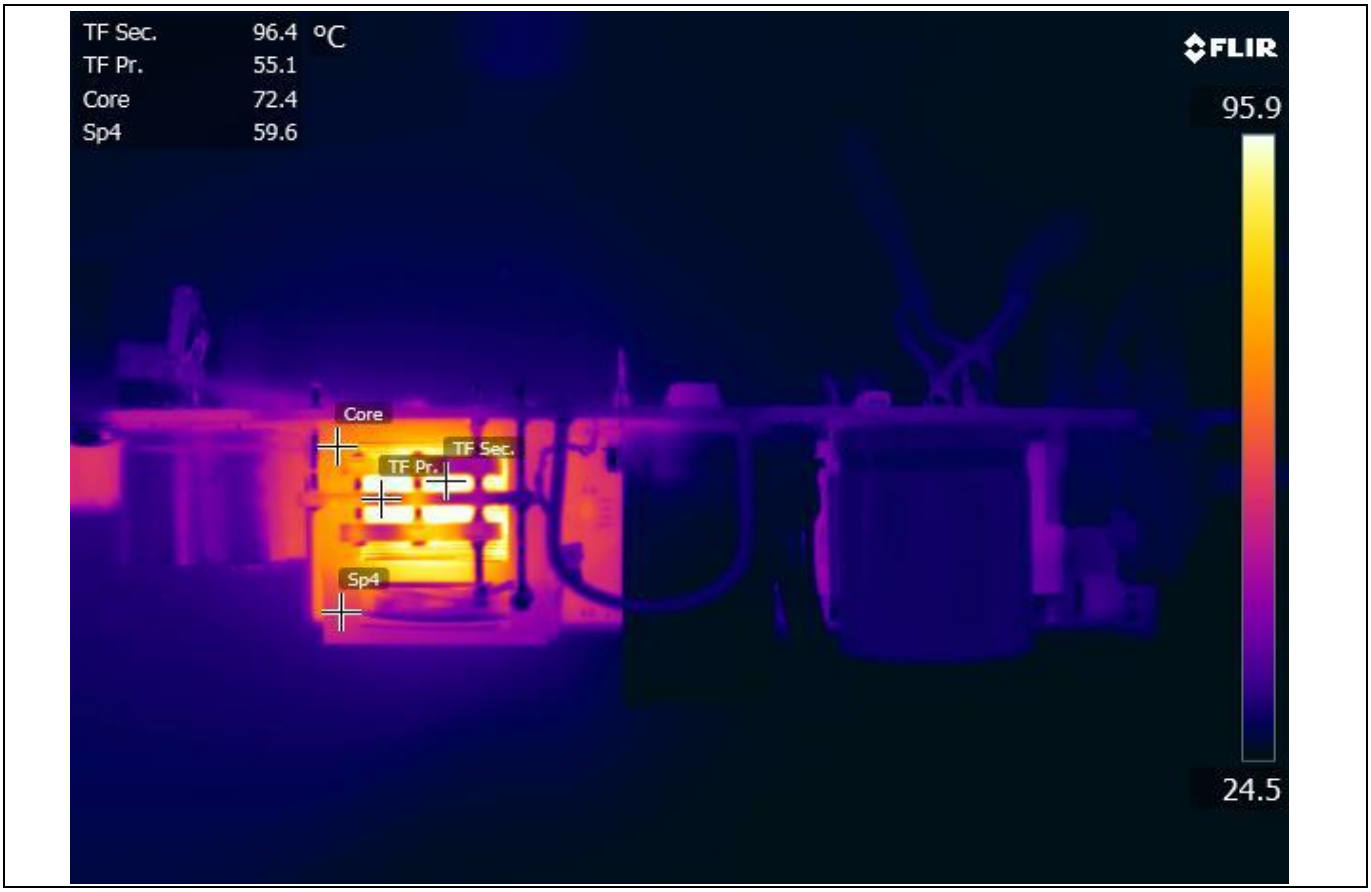


Figure 81 Main transformer detailed thermal map at 100 percent load (117 A) at room temperature (~24°C)

Finally it must be emphasized that the cooling is specifically designed in the present demo board in order to optimize the heat dissipation on the transformer, so special care must be taken with this aspect if the concept is transferred to general SMPS applications.

6 Conclusion

This document provides an overview of the Infineon 1400 W ZVS PSFB demo board based on the new 600 V CoolMOS™ CFD7 technology.

The design concept and the performance evaluation are described with a special focus on the key contribution of the CFD7 technology as an enabler of high efficiency combined with reliable operation across the whole load range, including the typical critical modes of this topology. In fact the demo board design is optimized for the 170 m Ω CFD7 device, namely IPP60R170CFD7.

An important contribution to the final excellent results also comes out of the applied digital control from the Infineon XMC4200. Two possible options, PCM and VM, are offered to the users for the converter control: these two are in fact the most popular in SMPS application of the PSFB topology. The applied control paths, on both the primary and secondary MOSFETs, with optimized delay time setting, enable an efficiency plot targeting the HV DC/DC stage of an 80Plus® Platinum® standard server power supply.

A GUI has been designed to help the user interact with the demo board: it enables the real-time reading of some key electrical parameters along with the possibility of carrying out design fine-tuning and protection monitoring.

The 1400 W demo board is realized in the same form factor as the 800 W version [15], which means with an almost 80 percent increased power density compared to the 800 W version. 800 W and 1400 W Infineon demo boards will cover two typical power ranges typically used in the server SMPS arena, using the modular approach very common today in order to take advantage of economies of scale. This is in fact one of the most important trends in HP SMPS applications. In order to achieve it the power density becomes a crucial requirement.

The planar main transformer with stacked resonant choke helps achieve the high power density of the demo board and results in minimized AC and core losses, and thus high efficiency across the entire load range, along with a perfect heat spread.

The final result is a robust and high-performance design able to fulfill all the general requirements for the HV DC/DC isolated stage of a server or industrial SMPS.

The present paper demonstrates that the ZVS PSFB topology is a valuable alternative to the LLC topology in addressing the 80Plus® Platinum® standard. A proper power device selection, both on the primary and secondary side, and an appropriate control, enable a good balance of performance, cost and reliability, avoiding all the pitfalls of a fully resonant approach, as in the LLC topology.

Further developments of the present design are already planned at Infineon.

The gate driving concept used for the HV MOSFETs on the primary side is going to be improved thanks to the introduction of the upcoming Infineon 2EDS family of driver ICs with reinforced isolation: this solution will replace the gate drive transformers and provide improved efficiency and reliability in even smaller outer dimensions.

7 Technical data package

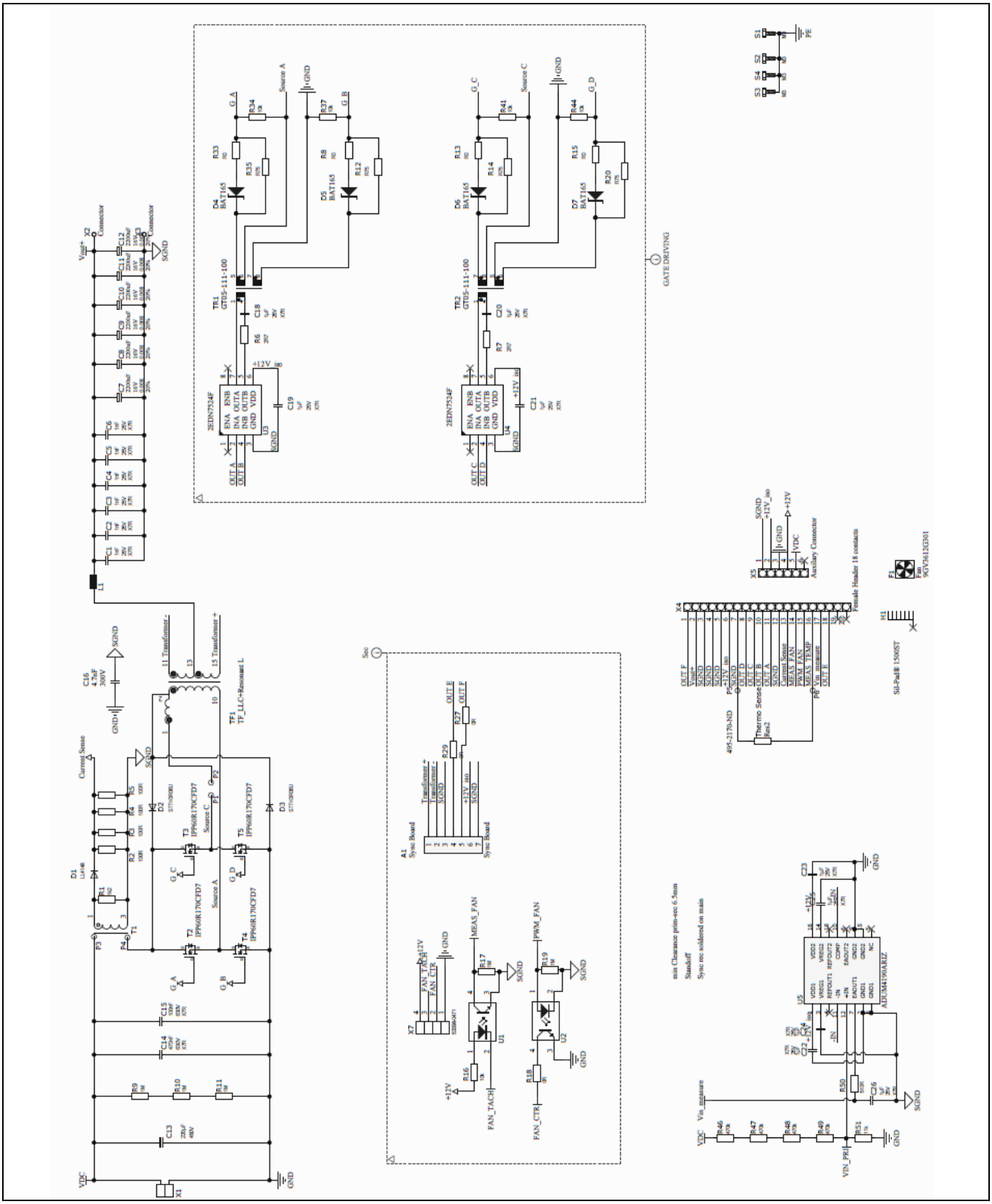


Figure 82 Main converter

BOM main board

Quantity	Designator	Comment	Value	Tolerance	Voltage	Footprint	Type	Supplier 1
6	C1, C2, C3, C4, C5, C6	SMT	1 nF		25 V	CAP1206R	Ceramic capacitor	Farnell
6	C7, C8, C9, C10, C11, C12	THT	2200 µF	20%	16 V	C_Aluminium Elektrolyt 10 mm V2	Electrolytic capacitor	Digi-Key
1	C13	THT	220 µF		450 V	C_Aluminium Elektrolyt 10 mm V4	Polarized capacitor	Digi-Key
1	C14	THT	470 nF		630 V	C_Foil Capacitor 10 mm grid V3	Ceramic capacitor	Farnell
1	C15	SMD	100 nF		630 V	CAP1812R	Ceramic capacitor	Farnell
1	C16	THT	4.7 nF	Y2	300 V	CAP-DISC 7.5 mm lead space	Ceramic capacitor	Farnell
9	C18, C19, C20, C21, C22, C23, C24, C25, C26	SMD	1 µF		25 V	CAP0805R	Ceramic capacitor	
1	D1	SMD	LL4148			DIOMELF3516N-0	Standard diode	Farnell
2	D2, D3	SMD	STTH3R06U			SMB/DO-214AA	Standard diode	Digi-Key
4	D4, D5, D6, D7	SMD	BAT165			S0D250X125X110-2N	Medium power AF Schottky diode	
1	F1	Fan	9GV3612G301			Fan_40×40×20 mm	SANYO DENKI - SANACE FANS 9GV3612G301	Farnell
1	H1	Heatsink	0S529			Heatsink AAVID 0S529 black anodized	Heatsink Aavid S529	Aavid
1	L1	THT	Output choke			Inductor Magnetics C058930A2 - V3	Inductor	ICE

1	R1	SMD	1k2	1%		RES1206R	Resistor	
2	R2, R3	SMD	100 R	1%		RES1206R	Resistor	
2	R6, R7	SMD	2R7	1%		RES0805R	Resistor	
4	R8, R13, R15, R33	SMD	0 R	1%		RES0805R	Resistor	
3	R9, R10, R11	SMD	1 M	1%		RES1206R	Resistor	
4	R12, R14, R20, R35	SMD	75 R	1%		RES0805R	Resistor	
1	R16	SMD	10 k	1%		RES0805R	Resistor	
2	R17, R19	SMD	1 M	1%		RES0805R	Resistor	
1	R18	SMD	0 R	1%		RES0805R	Resistor	
2	R27, R29	SMD	0 R	1%		RES1206R	Resistor	
4	R34, R37, R41, R44	SMD	10 k	1%		RES0603R	Resistor	
4	R46, R47, R48, R49	SMD	470 k	1%		RES0805R	Resistor	
1	R50	SMD	510 R	1%		RES0805R	Resistor	
1	R51	SMD	11 k	1%		RES0805R	Resistor	
4	S1, S2, S3, S4	THT	M3			M3	Screw	Farnell
1	T1	THT				CS transformer server Murata	WE-CST CS Transformer	Digi-Key
4	T2, T3, T4, T5	THT	IPP60R170CFD7			TO220_V	NMOS FET	
1	TF1	THT				Transformer Payton		Payton
1	Thermo Sense	THT				AXIAL-0.4	Resistor	Digi-Key
2	TR1, TR2	SMD	GT05-111-100			Transformer ICE	Pulse transformer	
2	U1, U2	SMD	VISHAY SFH6186-2			DIL-4-SMD	Optocoupler	Farnell
2	U3, U4	SMD	2EDN7524F			SOIC127P600X175-8N-2	2EDN752x/2EDN852x	
1	U5	SMD				SOIC16	ADUM4190ARIZ	Mouser
1	X1	THT				Connector	Pin	Digi-Key

						Phoenix Contact 1714955	Header	
5	X5	Auxiliary connector	Bürklin 25F3020			Bias supply	Einlötbuchse LB0, 76	25F3020
1	X7	SMD	53398-0471			Molex pico blade, 4 pins	Pin header, 4 contacts	Farnell
2	X2, X3	THT	Lugsdirect.com B2A-PCB					Lugsdirect.com
4	Heatsink clip							Aavid
4	PCB stand-off	THT					HARWIN R 30-1002002 Abstandhalter	Farnell

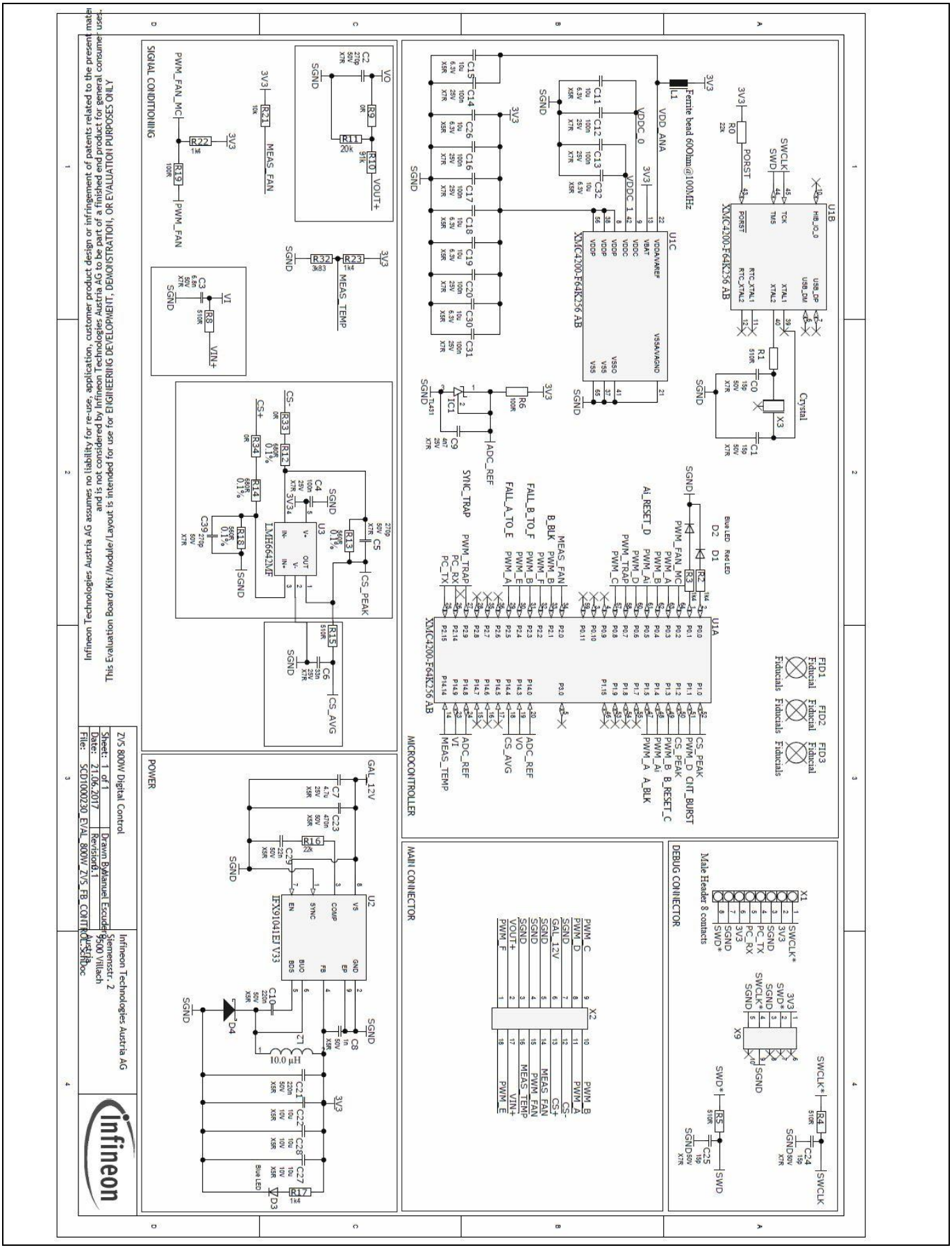


Figure 83 Control board

BOM control card

Quantity	Designator	Comment	Value	Tolerance	Voltage	Footprint	Type	Part number/ supplier
4	C0, C1, C24, C25	15 p	15 p	X7R	50 V	CAP0603R	Ceramic capacitor	732-7747-1-ND Digi-Key
3	C2, C5, C39	270 p	270 p	X7R	50 V	CAP0603R	Ceramic capacitor	
1	C3	6.8 n	6.8 n	X7R	50 V	CAP0603R	Ceramic capacitor	
8	C4, C12, C13, C14, C16, C17, C20, C31	100 n	100 n	X7R	25 V	CAP0603R	Ceramic capacitor	
1	C6	33 n	33 n	X7R	25 V	CAP0603R	Ceramic capacitor	
1	C7	4.7 µ	4.7 µ	X5R	25 V	CAP0805R	Ceramic capacitor	8126429 Farnell
1	C8	1 n	1 n	X5R	50 V	CAP0603R	Ceramic capacitor	
1	C9	4n7	4n7	X7R	25 V	CAP0603R	Ceramic capacitor	
2	C10, C21	220 n	220 n	X5R	50 V	CAP0805R	Ceramic capacitor	
10	C11, C15, C18, C19, C22, C26, C27, C28, C30, C32	10 µ	10 µ	X5R	6.3 V	CAP0805R	Ceramic capacitor	
1	C23	470 n	470 n	X5R	50 V	CAP0805R	Ceramic capacitor	
1	C29	22 n	22 n	X5R	50 V	CAP0603R	Ceramic capacitor	
1	D1	Red LED	Red LED			LED-0603R	LED	1685062 Farnell
2	D2, D3	Blue LED	Blue LED			LED-0603R	LED	1685096 Farnell
1	D4	DO-214-AA/SMB; 2 C-bend leads; body 5.3 × 3.6				SOD323	Schottky diode	2432677 Farnell

		mm, inc. leads (L × W)						
1	IC1	SMD	TL431			SOT23R	Integrated circuit	296-17328-2-ND Digi-Key
1	L1	Ferrite bead 60 Ω at 100 MHz	Ferrite bead 60 Ω at 100 MHz			RES0603R	Inductor	1635704 Farnell
1	L2	10.0 µH				WE-TPC 2828	SMD Shielded Tiny Power Inductor WE-TPC, L=10.0 µH	
2	R0, R16	22 k	22 k	1%		RES0603R	Resistor	
5	R1, R4, R5, R8, R15	510 R	510 R	1%		RES0603R	Resistor	
5	R2, R3, R17, R22, R23	1k4	1k4	1%		RES0603R	Resistor	
1	R6	SMD	100 R	1%		RES0603R	Resistor	
3	R9, R33, R34	0 R	0 R	1%		RES0603R	Resistor	
1	R10	91 k		1%		RES0603R		
1	R11	20 k		1%		RES0603R		
2	R12, R14	680 R	680 R	0.1%		RES0603R	Resistor	
2	R13, R18	560 R	560 R	0.1%		RES0603R	Resistor	
1	R19	100 R	100 R	1%		RES0603R	Resistor	
1	R21	10 k	10 k	1%		RES0603R	Resistor	
1	R32	3k83	3k83	1%		RES0603R	Resistor	

1	U1	XMC4200-F64K256 AB	XMC4200-F64K256 AB			INF-PG-LQFP-64-19-5800X5800TP_M	80 MHz XMC4200 MCU with 256 KByte program memory, 40 Kbyte SRAM, 3.3 V, -40°C to 125°C, PG-LQFP-64, green	2418736 Farnell
1	U2	IFX91041EJ V33		2(4)%		INF-PG-DSO-8-27_L	1.8 A DC/DC step-down voltage regulator, -40°C to 150°C, PG-DSO-8-27, reel, green	IFX91041EJV33INTR-ND Digi-Key
1	U3	LMH6642MF	LMH6642MF			SOT23-5	LMH664x low power, 130 MHz, 75 mA rail-to-rail output amplifiers	1468898RL Farnell
1	X1	Male header, 8 contacts				Female header, double row 2x4c	TSW-104-06-G-D	Samtec
1	X2					Connector 2 mm pCB 2 × 9 – V2	TMM-109-05-T-D	Samtec
1	X3	Crystal	Crystal oscillator			NX3225GD		1253-1151-2-ND Digi-Key
1	X9	SMD				FTSH-105-XX-X-DV-K	Pin header 2x5 contacts	SAM8799-ND Digi-Key

SR

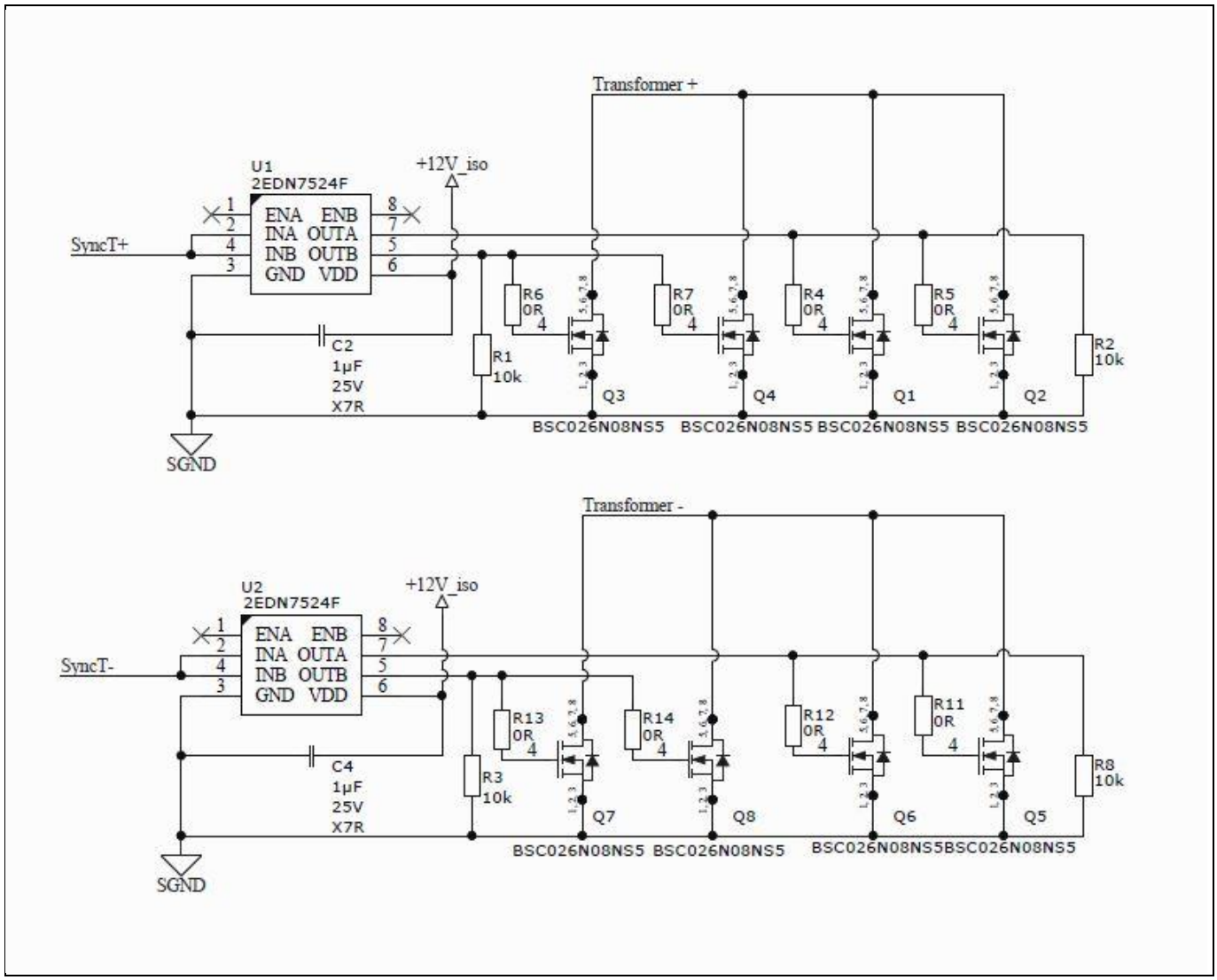


Figure 84 Synchronous rectification board

BOM

Quantity	Designator	Comment	Value	Tolerance	Voltage	Footprint	Description
2	C2, C4	Capacitor Ceramic	1 µF	X7R	25 V	CAP0805R	Capacitor cCeramic
8	Q1, Q2, Q3, Q4, Q5, Q6, Q7, Q8	BSC026N08NS5				SuperSO8	N-Channel OptiMOS™ 3 power-transistor, 40 V V_{DS}, 100 A ID, -55 to 150 degC, PG-TDSON-8-1, Reel, Green

4	R1, R2, R3, R8	Resistor	10 k	5%		RES0805R	Resistor
8	R4, R5, R6, R7, R11, R12, R13, R14	Resistor	0 R	5%		RES0805R	Resistor
2	U1, U2	2EDN7524F	2EDN7524F			SOIC127P600X175-8N-2	2EDN752x / 2EDN852x

8 Useful materials and links

In the following links, you can find more detailed information about the devices used from Infineon and the magnetic components.

- Primary HV MOSFETs CoolMOS™ IPP60R170CFD7

https://www.infineon.com/dgdl/Infineon-IPP60R170CFD7-DS-v02_00-EN.pdf?fileId=5546d4625e763904015ea3d82d3331b1

- Microcontroller XMC4200

https://www.infineon.com/dgdl/Infineon-XMC4100_XMC4200-DS-v01_02-en.pdf?fileId=db3a30433afc7e3e013b3cf9b2816573

- Advanced dual channel gate drive 2EDN7524F

https://www.infineon.com/cms/en/product/power/gate-driver-ics/non-isolated-gate-driver/eicedriver-2edn-gate-driver-for-discrete-mosfets/2EDN7524F/productType.html?productType=5546d4624cb7f111014d66f8aabc4fdc

- Bias converter controller CoolSET™ ICE5QSAG + CoolMOS™ IPU80R4K5P7

ICE5QSAG

IPU80R4K5P7

- SR MOSFETs OptiMOS™ BSC026N08NS5

https://www.infineon.com/cms/en/product/power/mosfet/20v-300v-n-channel-power-mosfet/80v-100v-n-channel-power-mosfet/BSC026N08NS5/productType.html?productType=5546d4624ad04ef9014addb223cb7a23

- Planar magnetics by Payton (main transformer and resonant choke)

http://www.paytongroup.com/1263

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10 List of abbreviations

Abbreviation	Definition
ADC	Analog to Digital Converter
BD	Body Diode
BOM	Bill of Materials
CAD	Computer-Aided Design
CCU	Capture and Compare Unit
CLT	Coreless Transformer
CMTI	Common Mode Transient Immunity
C_{oss}	Output capacitance C_{oss} = CDS + CGD
$C_{o(tr)}$	Effective output capacitance, time related
COM	Communication port
C_r	Resonant capacitance
CSG	Comparator and Slope Generator
DAC	Digital to Analog Converter
DC	Direct Current
DMA	Direct Memory Access
DSP	Digital Signal Proccesor
di/dt	Steepness of current slope at turn-off/turn-on
EEPROM	Electrically Erasable Programmable Read-Only Memory
EMI	Electromagnetic Interference
E_{oss}	Stored energy in output capacitance (C_{oss}) at typ. V_{DS} = 400 V
ERU	Event Request Unit
FET	Field Effect Transistor
FPU	Floating Point Unit
F_{sw}	Switching frequency
GaN	Gallium nitride
GND	Electric ground
GUI	Graphical User Interface
HB	Half-Bridge
HS	High-Side
HRC	High Resolution Channel
HRPWM	High Resolution PWM
HV	High Voltage
IC	Integrated Circuit
I_D	Drain-to-source current
IDE	Integrated Development Environment
I_{out_phase}	Output current of one converter
I_{res}	Resonant current

List of abbreviations

Abbreviation	Definition
I^2C	Inter-integrated circuit communication protocol
LCD TV	Liquid Crystal Display Television
L_r	Resonant inductance
L_m	Magnetizing inductance
LS	Low-Side
LV	Low Voltage
MAC	Multiplication and accumulation unit
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
NTC	Negative Temperature Coefficient thermistor
OCP	Over-Current Protection
PFC	Power Factor Correction
PI	Proportional Integral controller
PSU	Power Supply Unit
PWM	Pulse Width Modulation
Q_G	Gate charge
Q_{oss}	Charge stored in the C_{oss}
QR	Quasi Resonant
RAM	Random Access Memory
$R_{DS(on)}$	Drain-source on-state resistance
$R_{G,on/off}$	Gate resistor applied at on and off transitions
SMPS	Switched Mode Power Supply
SPI	Serial Peripheral Interface
SR	Synchronous Rectification
SW	Software
TDP	Technical Data Package
TTL	Transistor-Transistor Logic
UART	Universal Asynchronous Receiver-Transmitter
USB	Universal Serial Bus
USIC	Universal Serial Interface Channel
V_{Bulk}	Bulk capacitor voltage
V_{cc}	Supply voltage
V_{Cr}	Resonant capacitor voltage
V_{DS}	Drain-to-source voltage
V_{GS}	Gate-to-source voltage
$V_{O;PFC}$	PFC output voltage
V_{out}	Output voltage
ZVS	Zero Voltage Switching
ZVS PSFB	Zero Voltage Switching Phase Shift Full Bridge

Revision history

Document version	Date of release	Description of changes

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